

A Tutorial on Phase Noise

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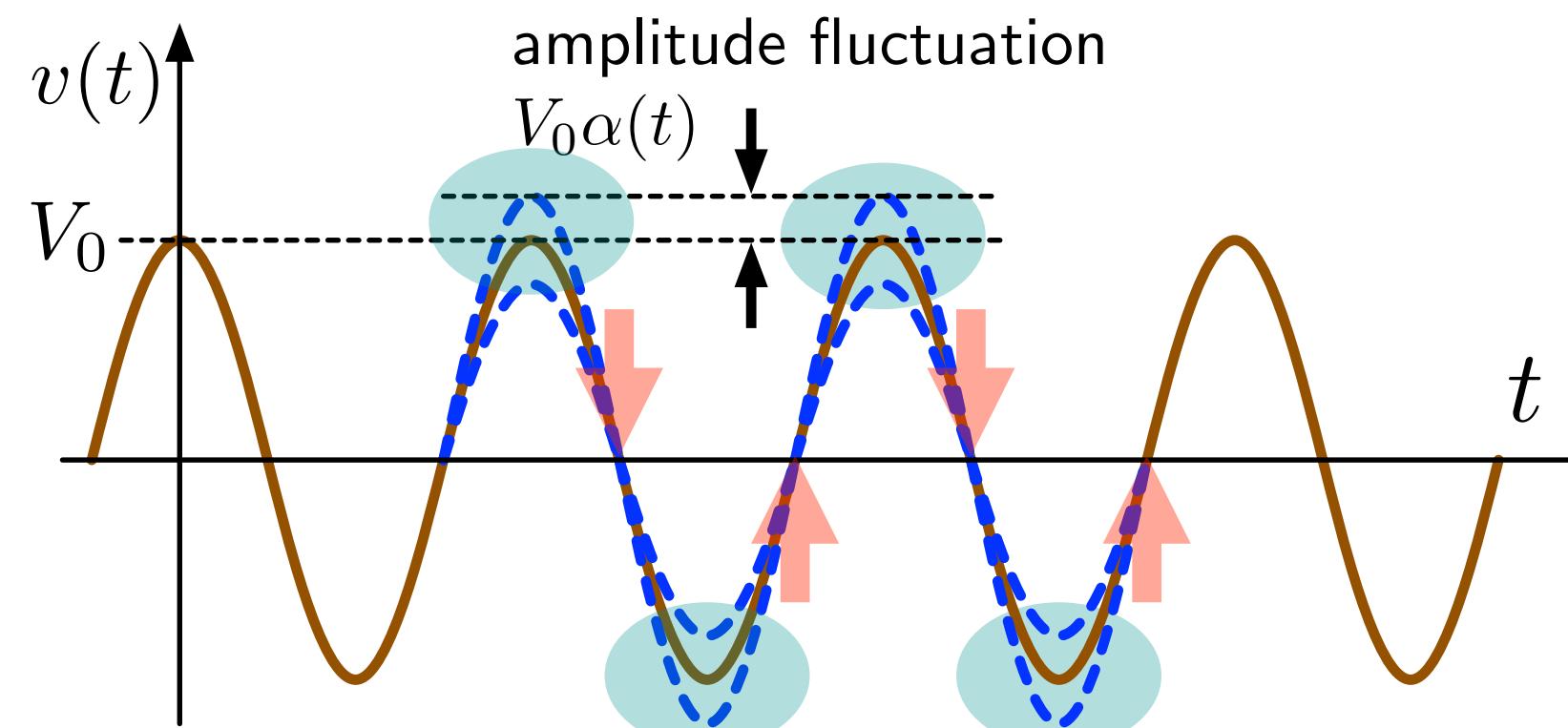
Outline

- Clock signal, phase noise, and friends
- The measurement of phase noise
- Digital circuits
- Additional facts
- Frequency synthesis
- ADCs
- Time-to-digital conversion
- ...and something more

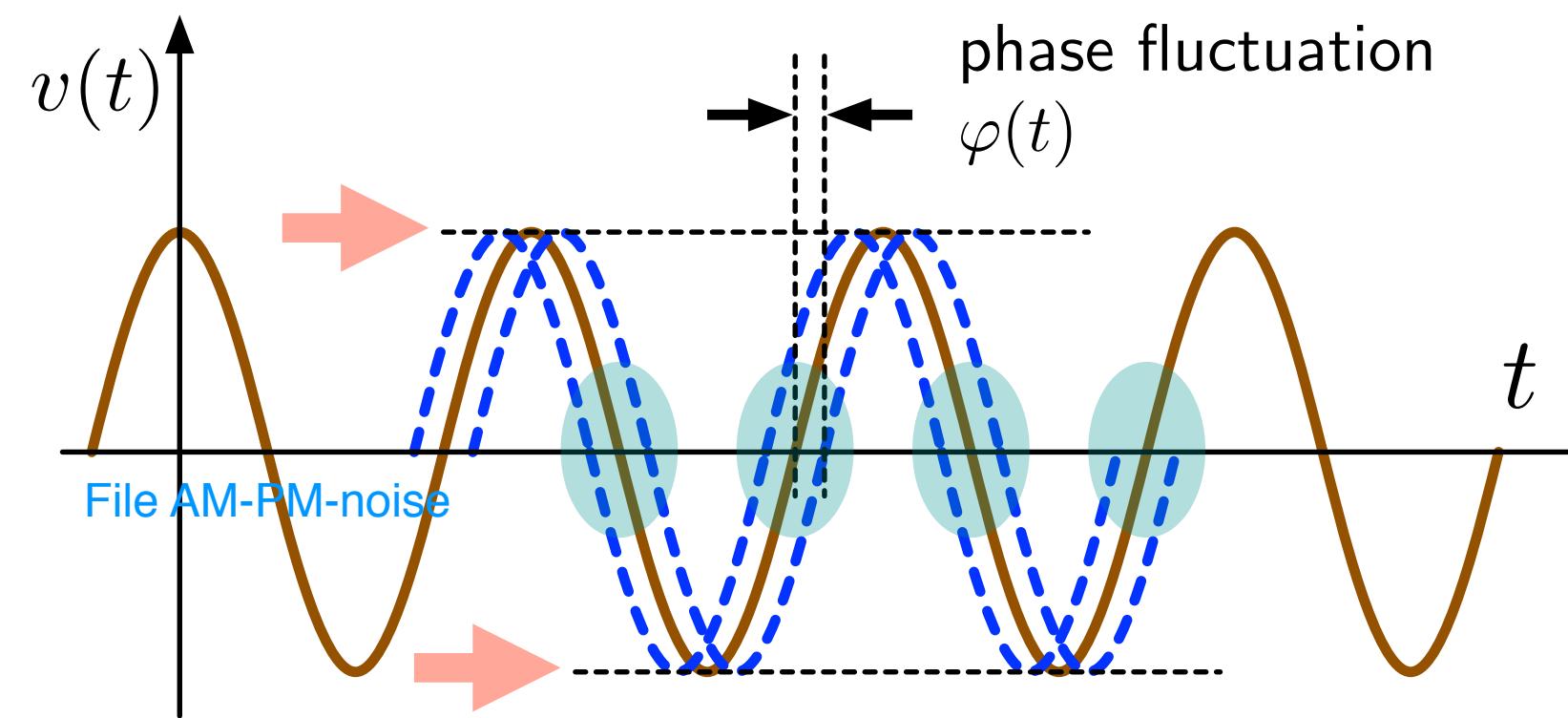
home page <http://rubiola.org>

The Clock Signal

amplitude fluctuation



phase fluctuation



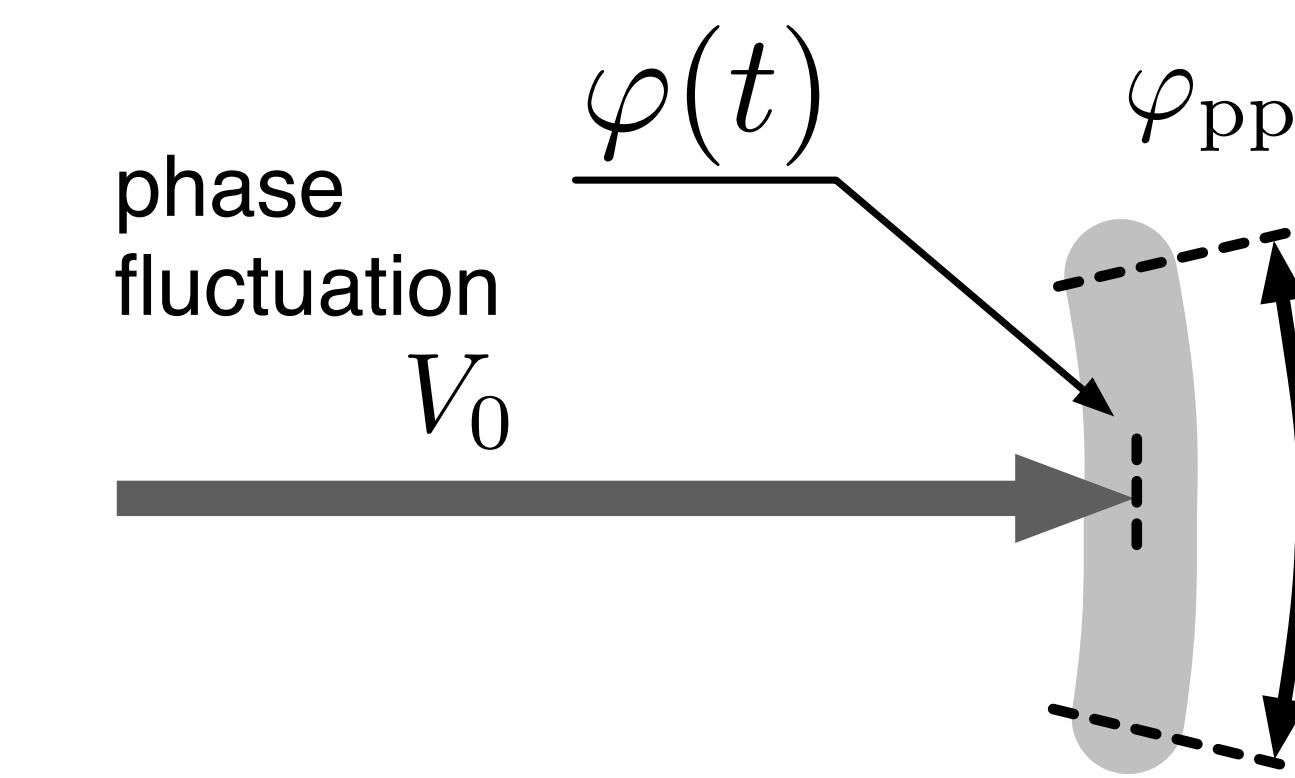
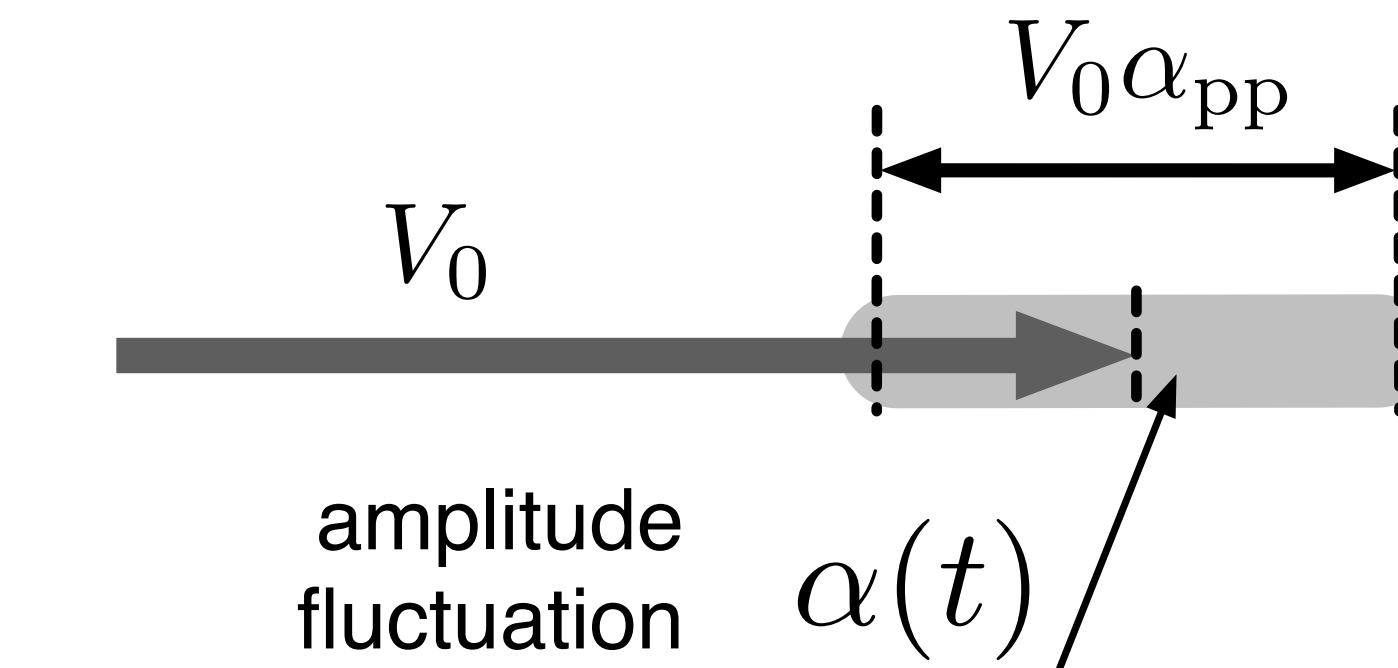
polar coordinates

$$v(t) = V_0 [1 + \alpha(t)] \cos [\omega_0 t + \varphi(t)]$$

Cartesian coordinates $v(t) = V_0 \cos \omega_0 t + n_c(t) \cos \omega_0 t - n_s(t) \sin \omega_0 t$

under low noise approximation

$$|n_c(t)| \ll V_0 \quad \text{and} \quad |n_s(t)| \ll V_0$$



It holds that

$$\alpha(t) = \frac{n_c(t)}{V_0} \quad \text{and} \quad \varphi(t) = \frac{n_s(t)}{V_0}$$

$S_\varphi(f)$ and $\mathcal{L}(f)$

Definition of $S_\varphi(f)$

Autocovariance

$$S_\varphi(f) = 2 \mathcal{F} \{C_{\varphi\varphi}(\tau)\}, f > 0$$

WK theorem

$$S_\varphi(f) = 2 \mathbb{E} \{\Phi(f)\Phi^*(f)\}, f > 0$$

measured

$$S_\varphi(f) \approx \frac{2}{T} \langle \Phi(f)\Phi^*(f) \rangle_m, f > 0$$

$S_\varphi \rightarrow [\text{rad}^2/\text{Hz}]$

$10 \log_{10}(S_\varphi) \rightarrow [\text{dB}\text{rad}^2/\text{Hz}]$

Definition of $\mathcal{L}(f)$

The IEEE Std 1139-2009

$$\mathcal{L}(f) = \frac{1}{2} S_\varphi(f)$$

$$(\mathcal{L})_{\text{dB}} = (S_\varphi)_{\text{dB}} - 3 \text{ dB}$$

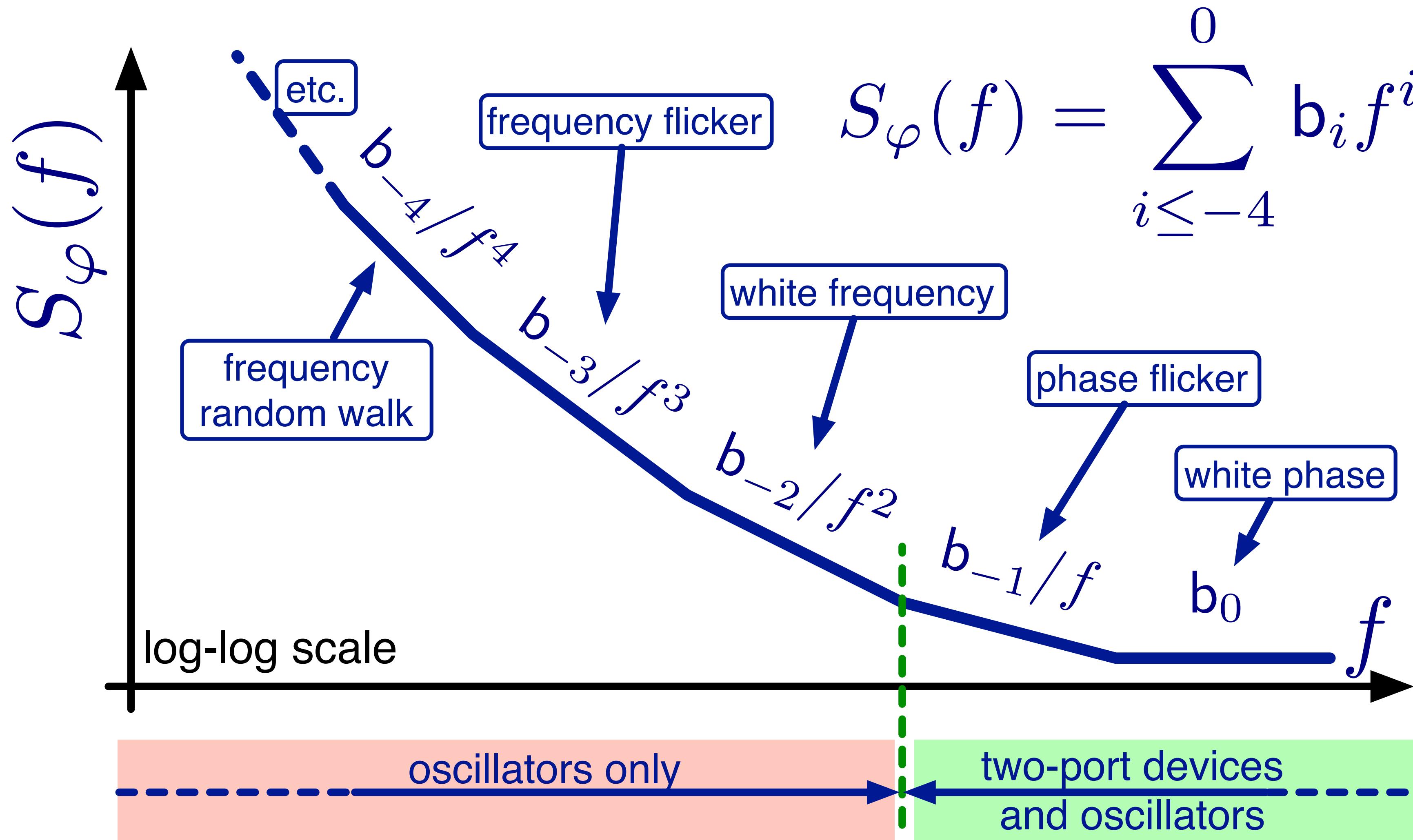
$10 \log_{10}(\mathcal{L}) \rightarrow [\text{dBc}/\text{Hz}]$

Unit of angle $\sqrt{2} \text{ rad} \approx 80^\circ$

Unwrapping the phase \rightarrow valid measures even for large angles (multiple cycles)

dBc no longer means (SSB noise / carrier)

Polynomial Law



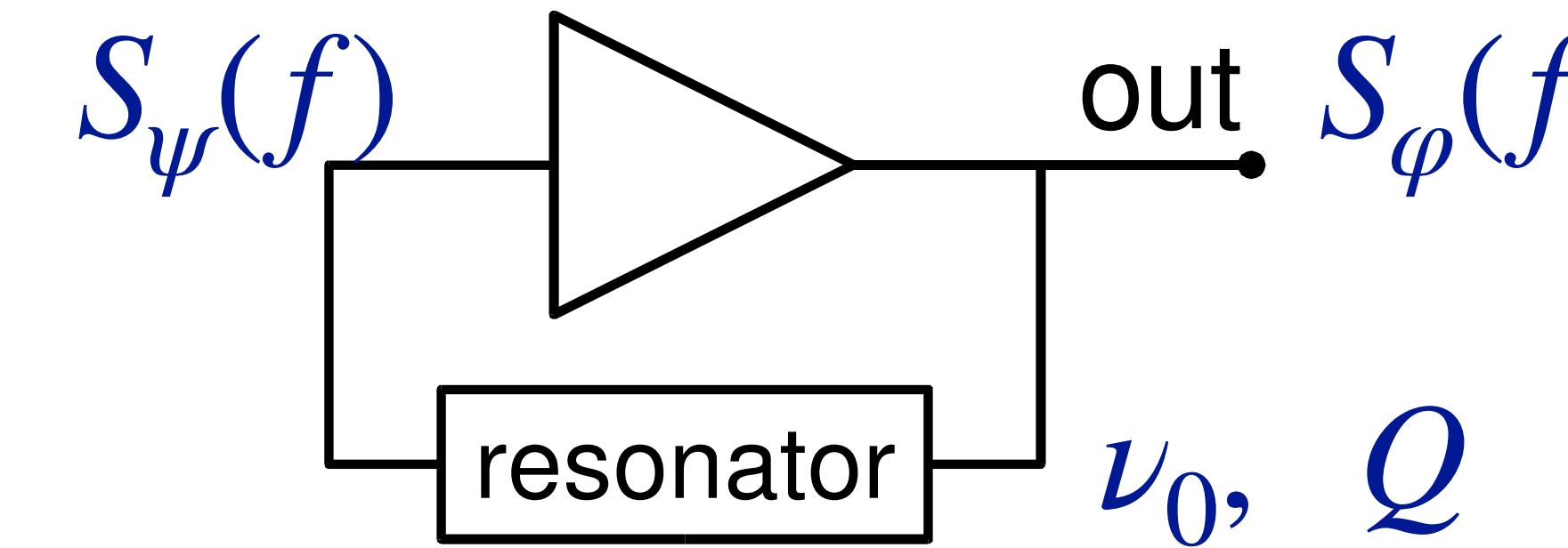
The integrated $1/f$ noise is amazingly small

$\ln(A_U/\tau_P) \simeq 140$ (21.5dB)

The Leeson Effect in a Nutshell

David B. Leeson, Proc. IEEE 54(2) p.329, Feb 1966

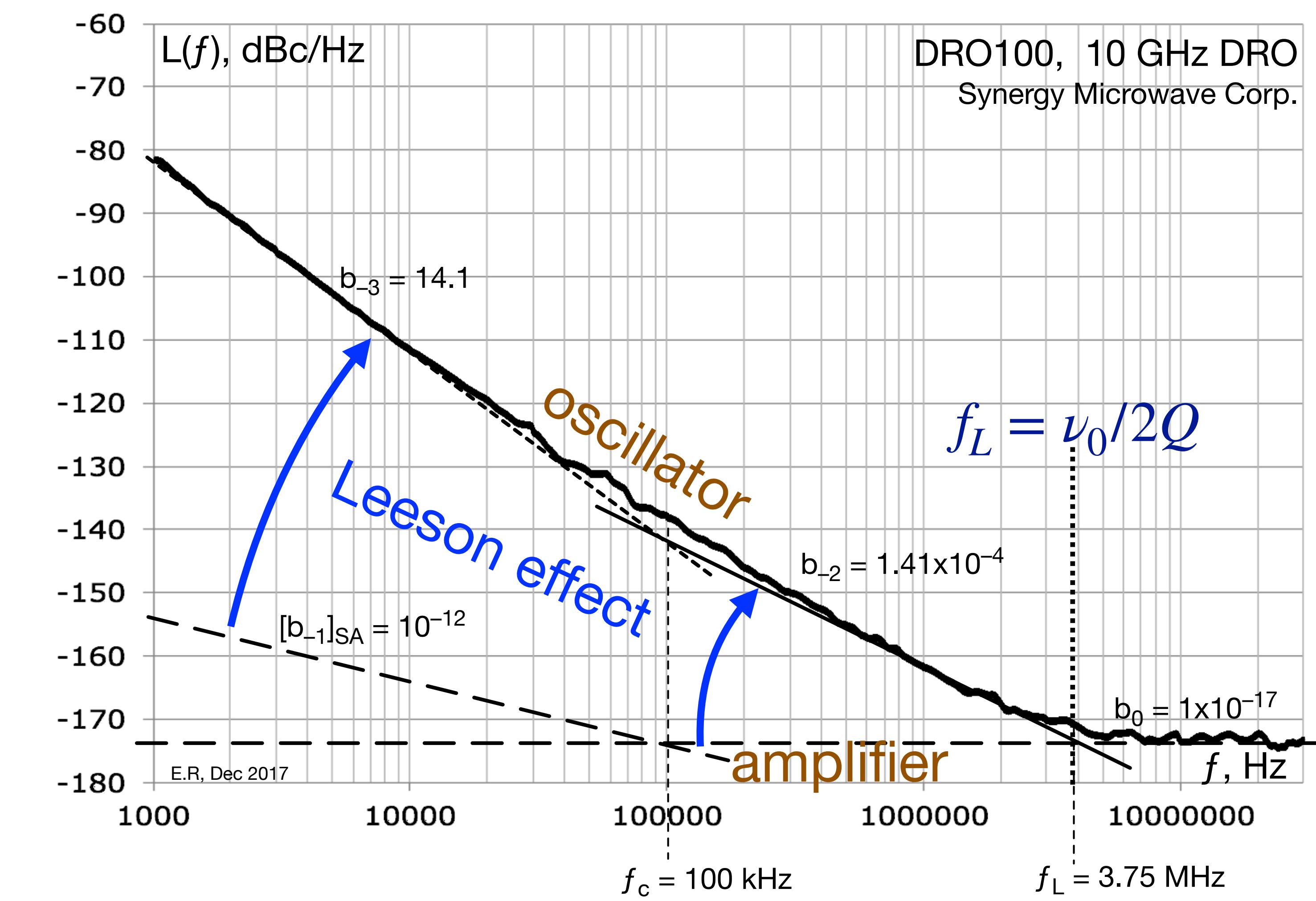
E. Rubiola, *Phase Noise and Frequency Stability in Oscillators*, Cambridge 2008, 2012



$$S_\varphi(f) = \left[1 + \left(\frac{\nu_0}{2Q} \right)^2 \frac{1}{f^2} \right] S_\psi(f)$$

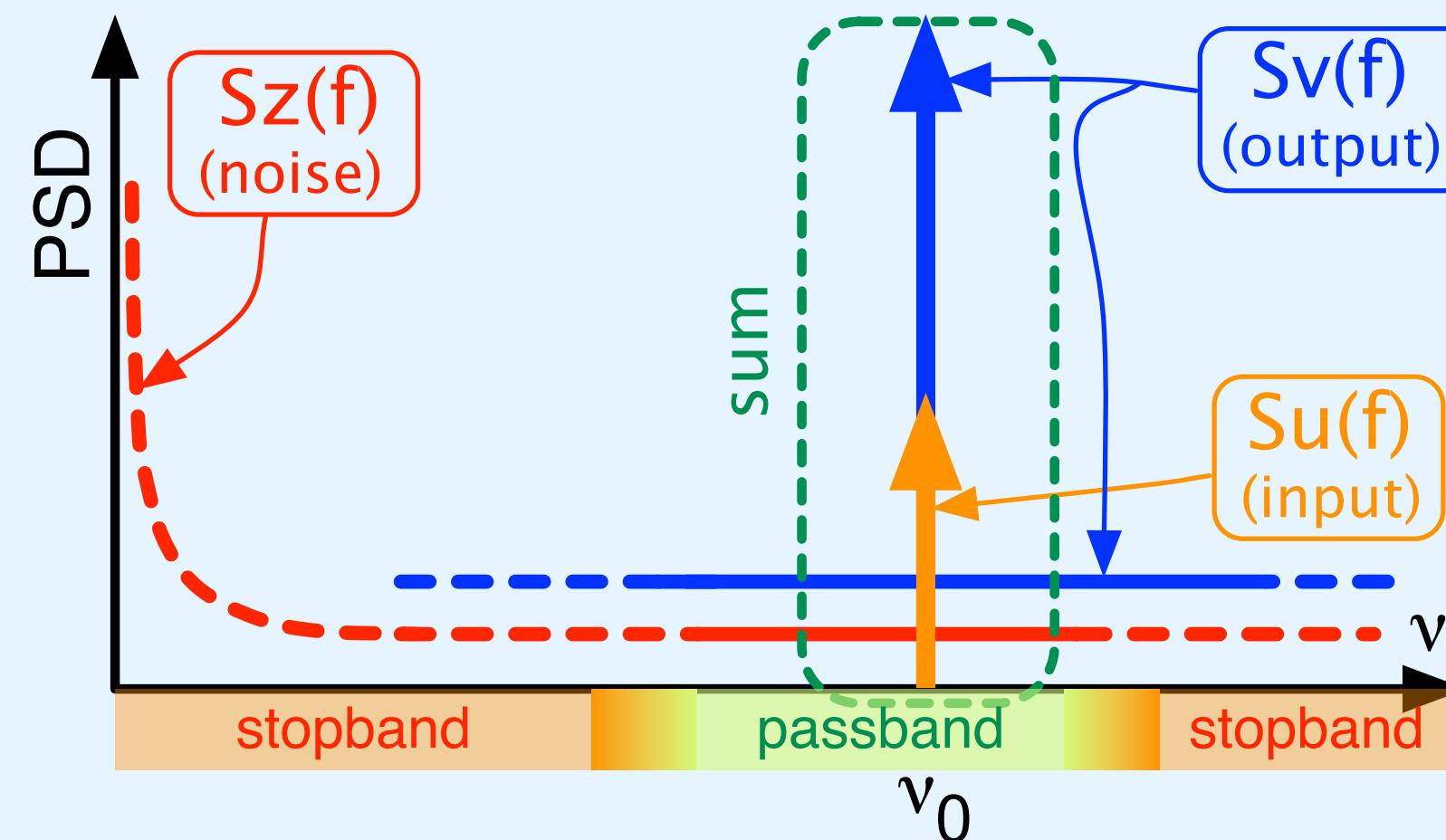
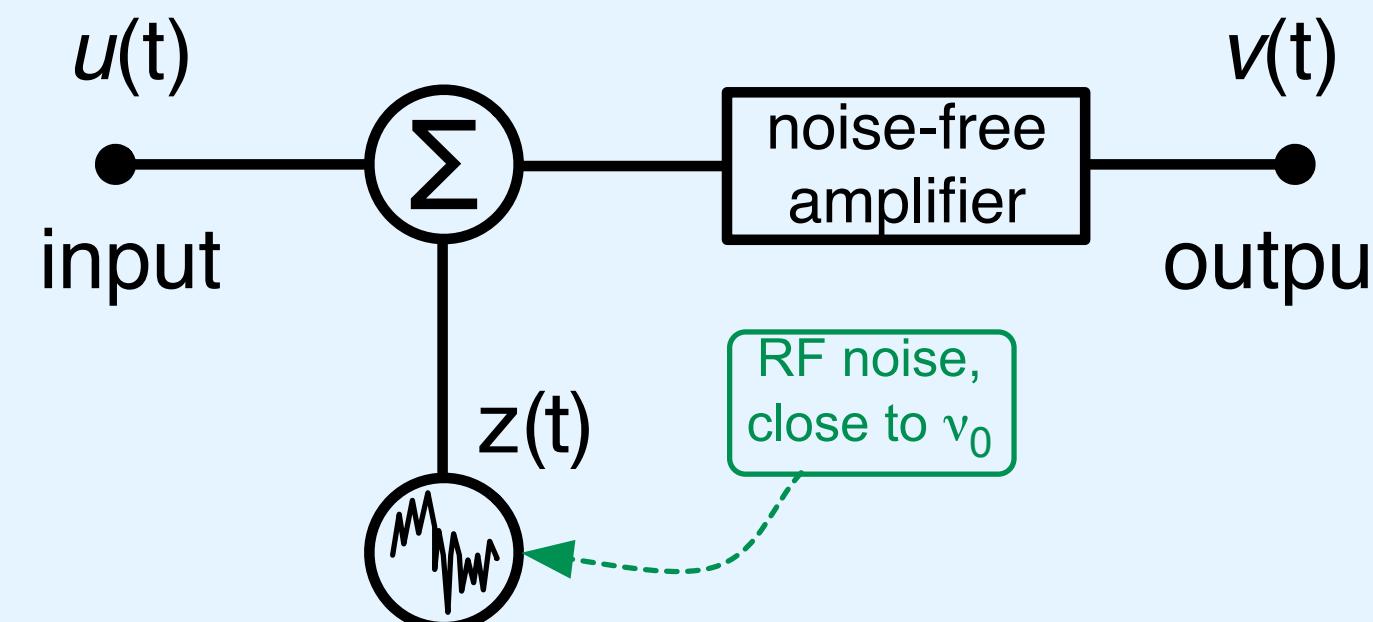
oscillator noise oscillator noise

Leeson effect



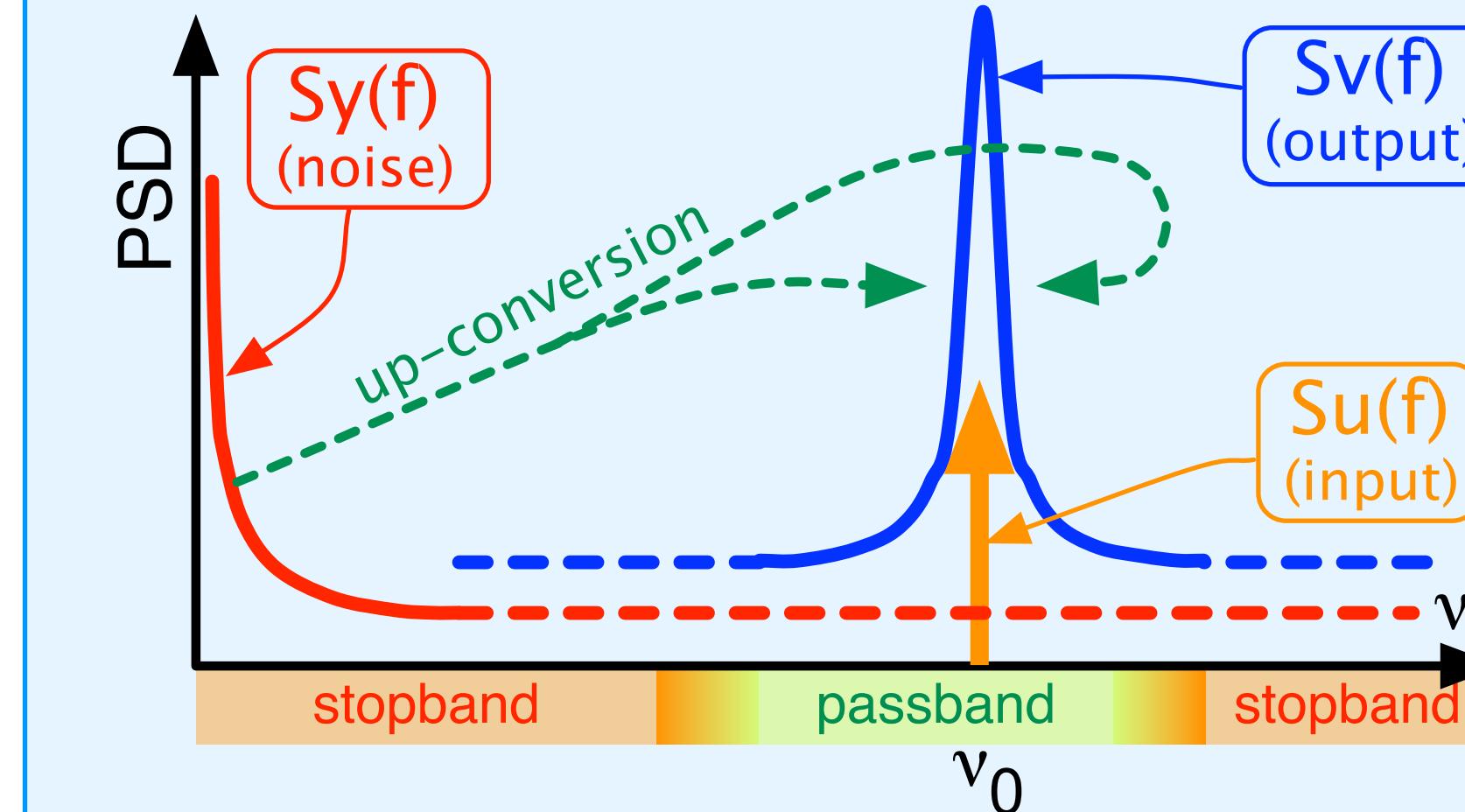
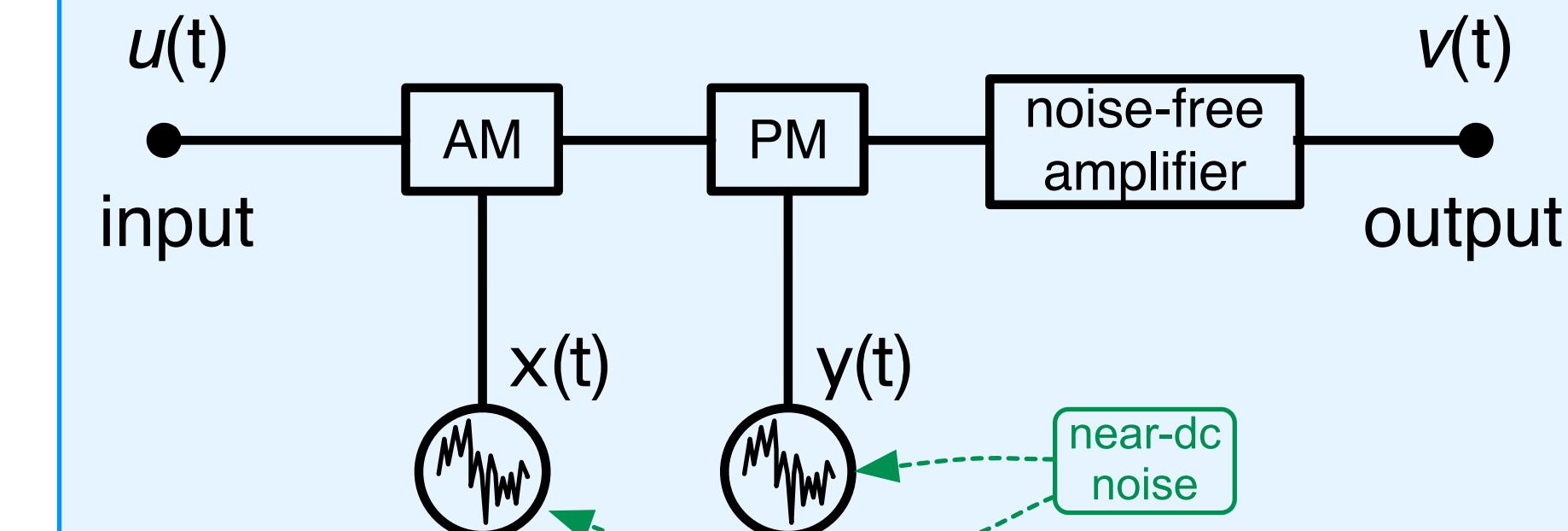
Additive vs Parametric Noise

additive noise



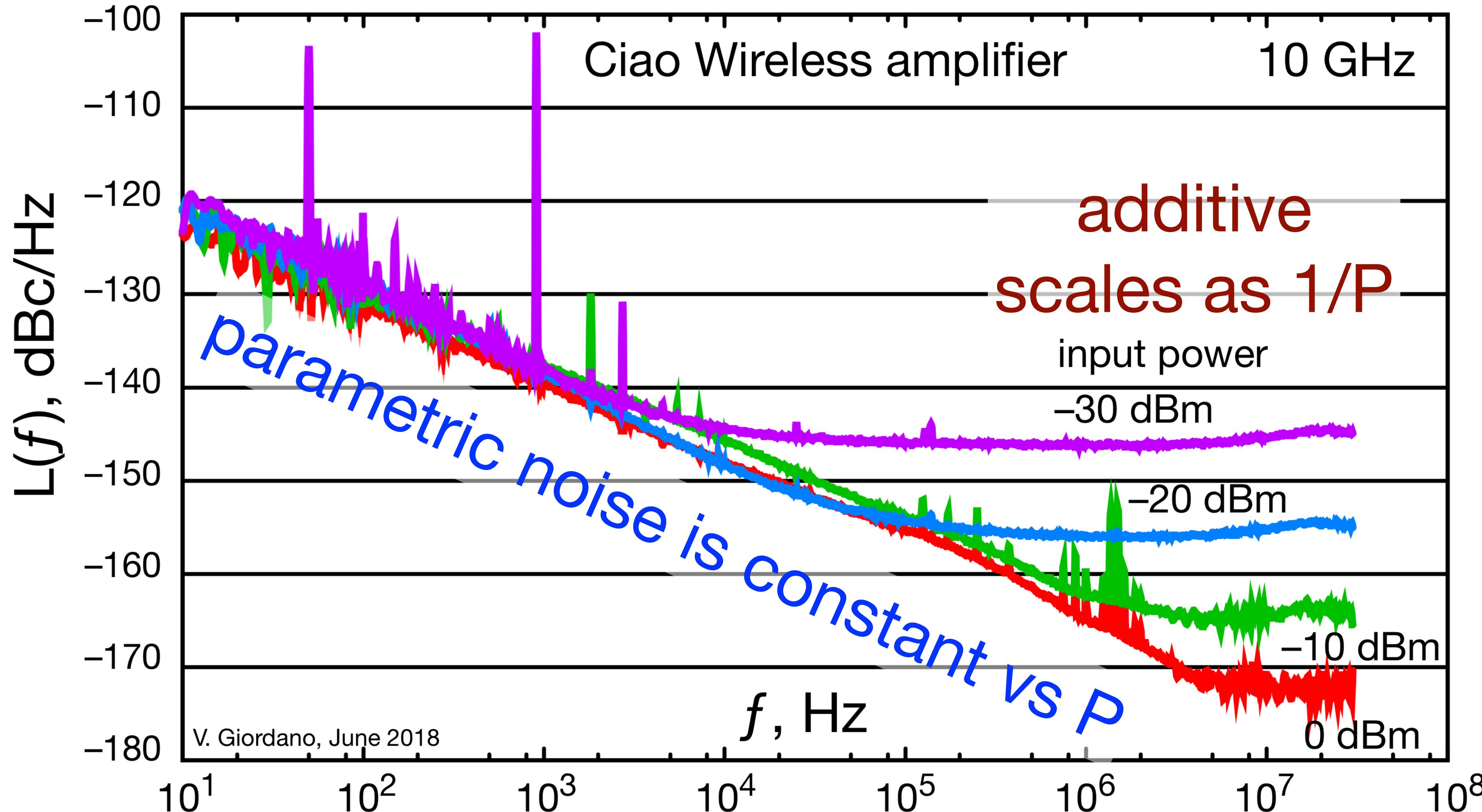
the noise sidebands are
independent of the carrier

parametric noise



the noise sidebands are
proportional to the carrier

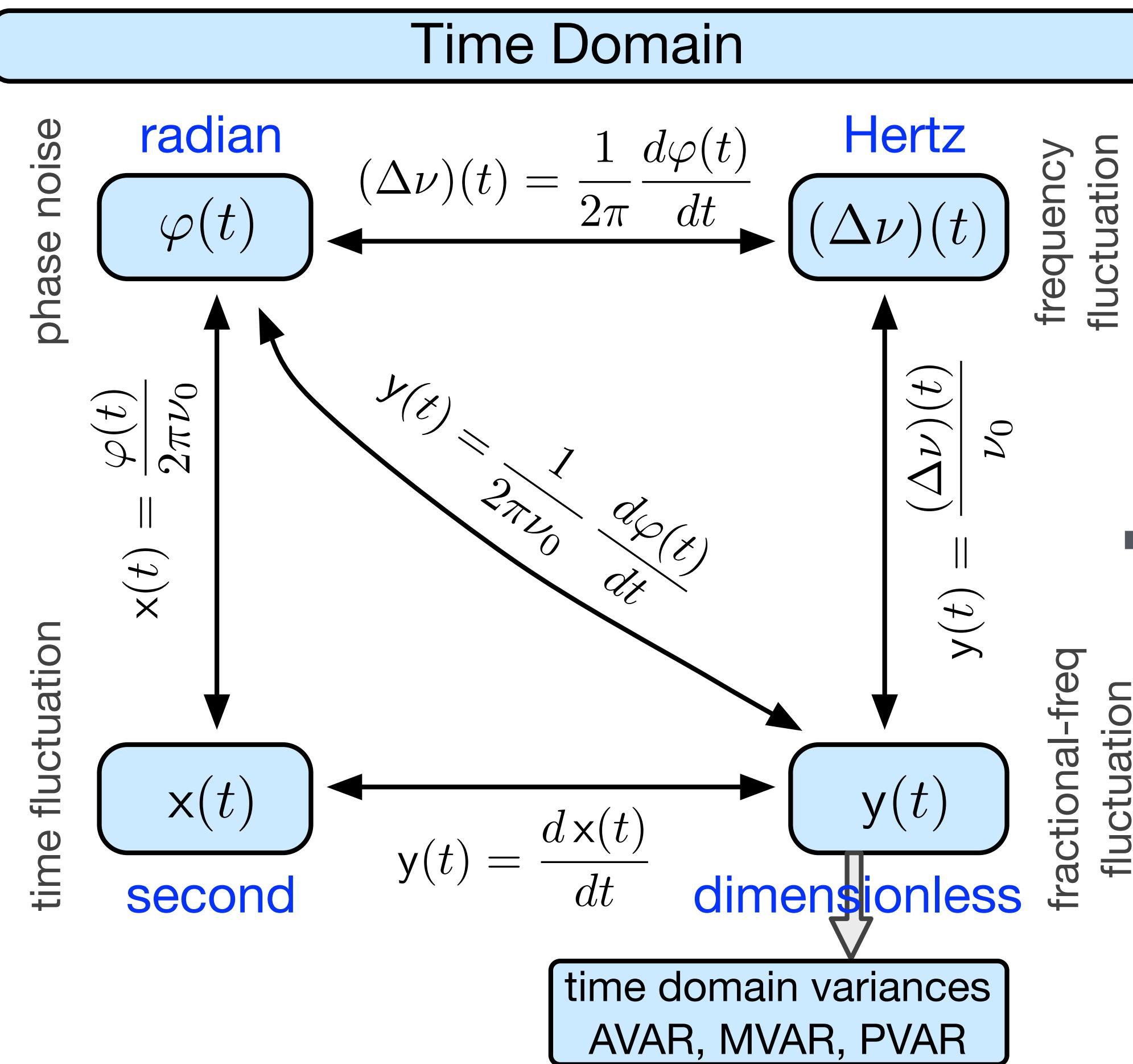
Example – Microwave Amplifier



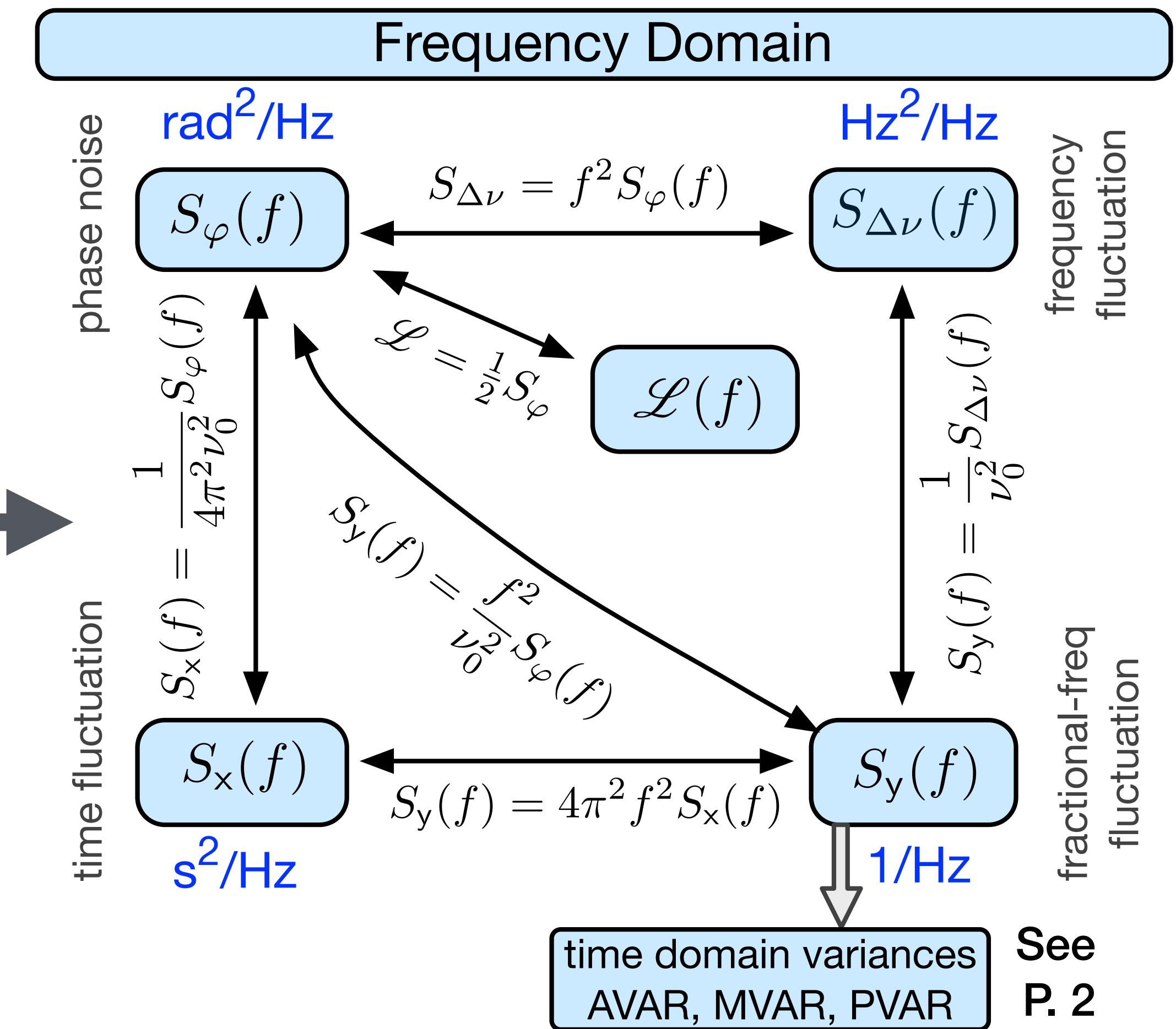
Parametric noise in amplifiers tends to be independent of ν_0

Physical Quantities

Function of time (time series)



Power Spectral Density



boldface notation

total = nominal + fluctuation

$\varphi(t) = 2\pi\nu_0 t + \varphi(t)$ phase

$\nu(t) = \nu_0 + (\Delta\nu)(t)$ frequency

$\mathbf{x}(t) = t + \mathbf{x}(t)$ time

$\mathbf{y}(t) = 1 + \mathbf{y}(t)$ fractional frequency

Two Types of Noise Mechanism

Phase-type noise

- Phase noise $S_\varphi(f)$ is independent of ν_0
- Time fluctuation $S_x(f)$ scales as $1/\nu_0^2$

$$S_x(f) = \frac{1}{4\pi^2\nu_0^2} S_\varphi(f)$$

Time-type noise

- Time fluctuation $S_x(f)$ is independent of ν_0
- Phase noise $S_\varphi(f)$ scales as ν_0^2

Allan-(Like) Variance(s)

$y(t)$ = fractional frequency fluctuation

average $\bar{y} = \frac{1}{\tau} \int_{t_0}^{t_0+\tau} y(t) dt$

definition (AVAR)

$$\sigma_y^2(\tau) = \mathbb{E} \left\{ \frac{1}{2} [\bar{y}_2 - \bar{y}_1]^2 \right\}$$

same as the experimental variance with 2 samples

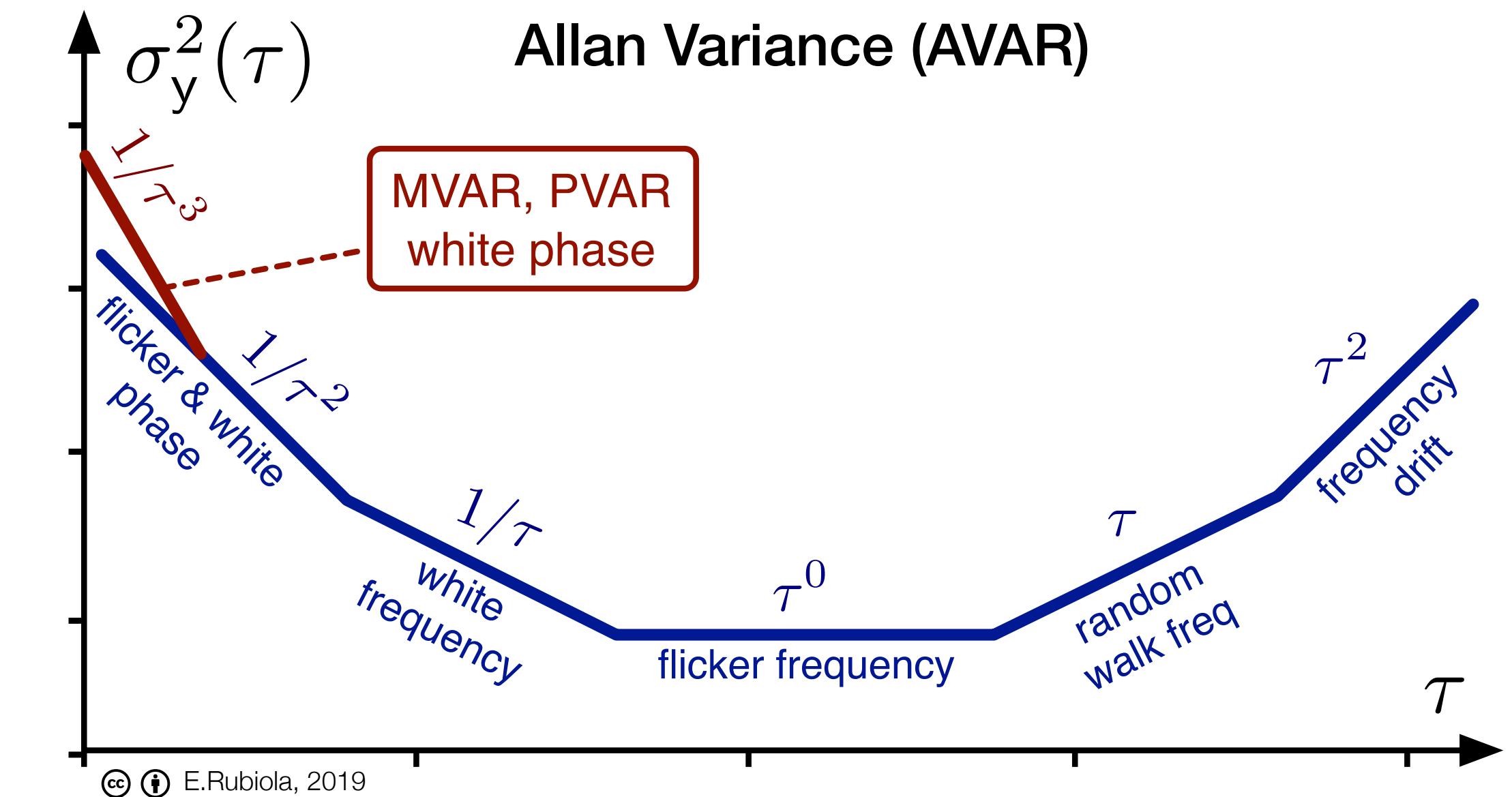
Expectation \rightarrow average on m samples

$$\sigma_y^2(\tau) = \frac{1}{m} \sum_{k=0}^{m-1} \frac{1}{2} [\bar{y}_{k+1} - \bar{y}_k]^2$$

E. Rubiola, RSI 76(5) 054703, May 2005

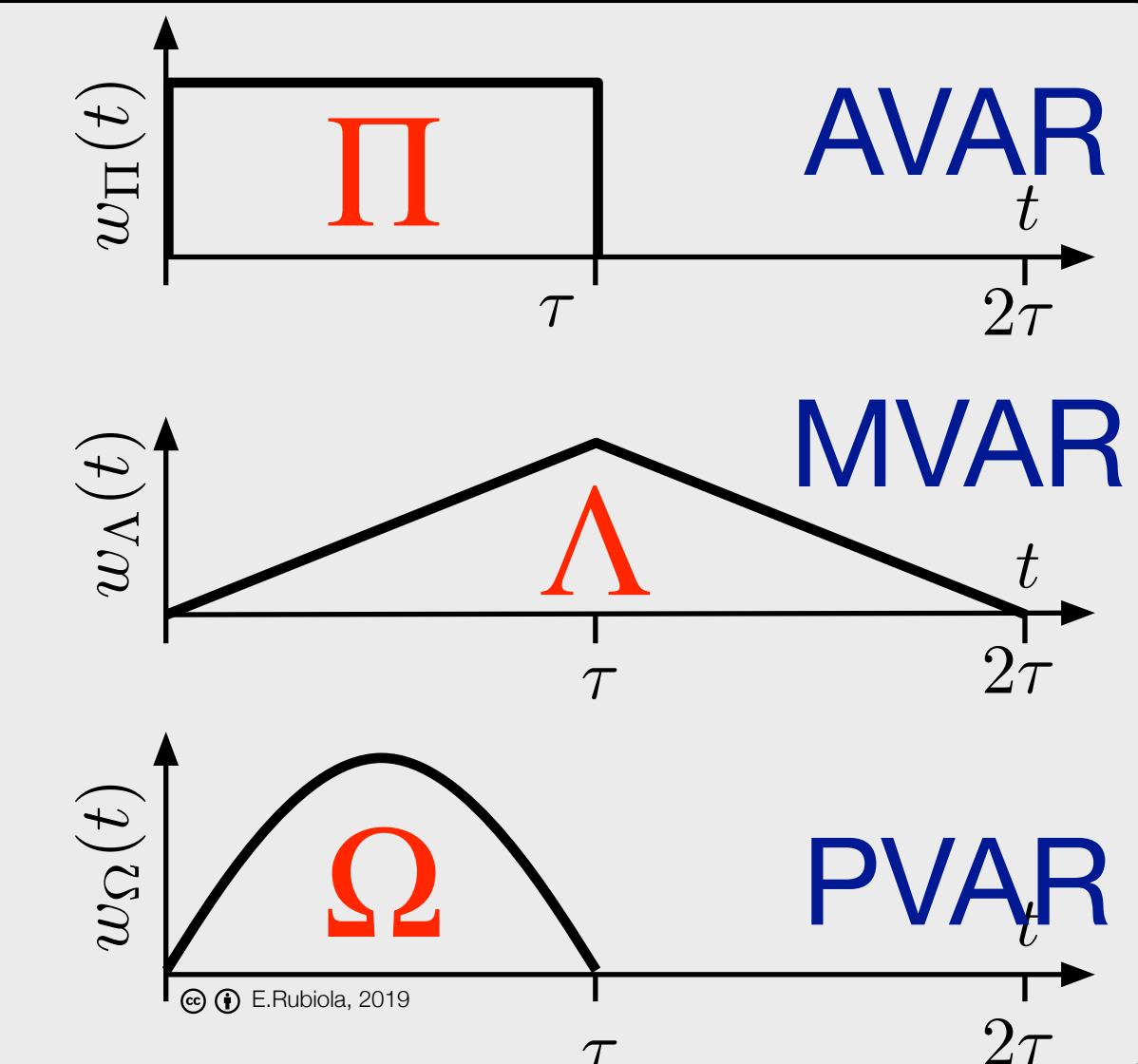
E. Rubiola & al, IEEE T UFFC 63(7) p.961, Jul 2016

F. Vernotte & al, IEEE T UFFC 63(4) p.611, Apr 2016



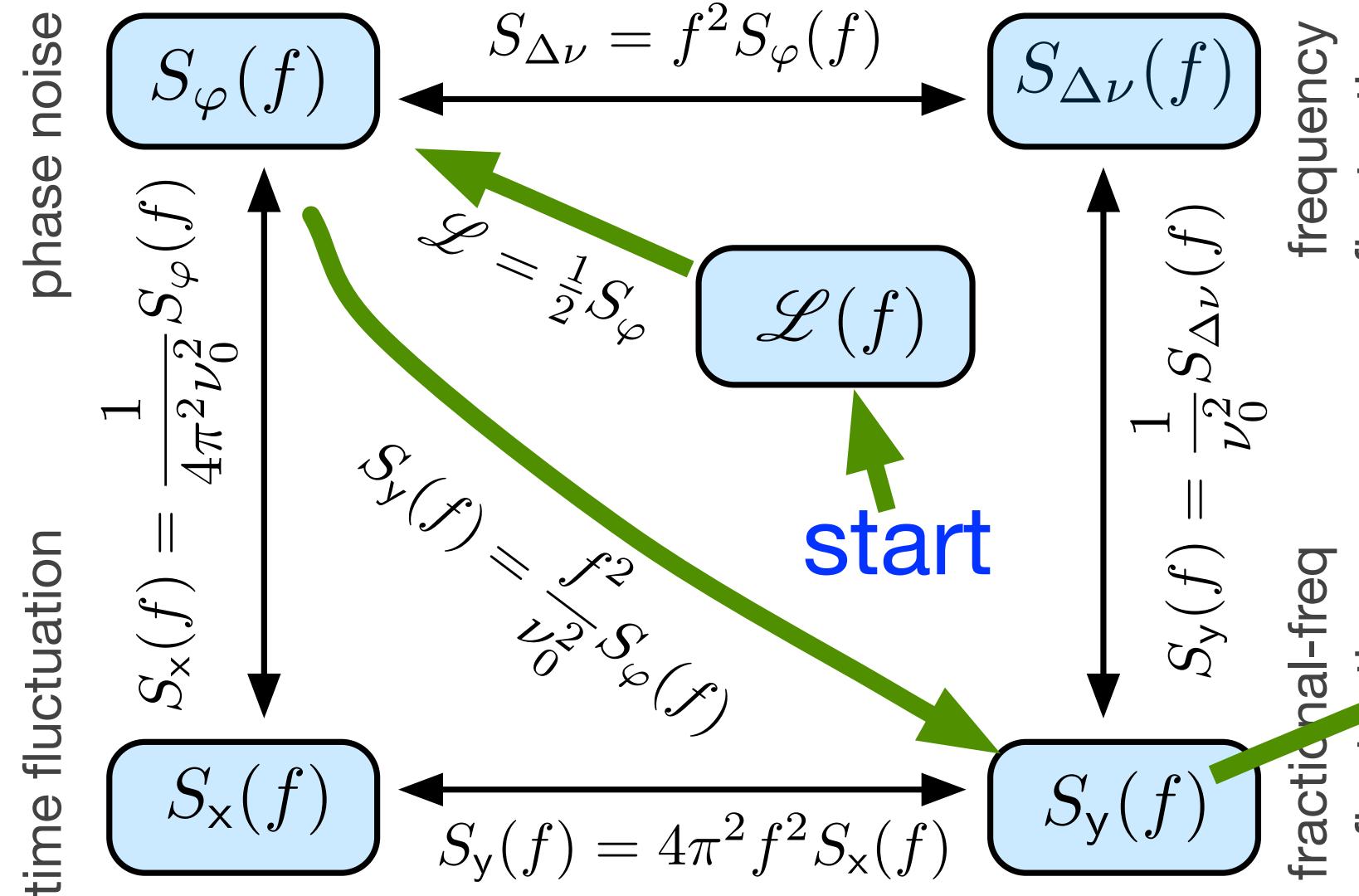
Use the weighted average

$$\bar{y} = \int_{\mathbb{R}} y(t) w(t) dr$$

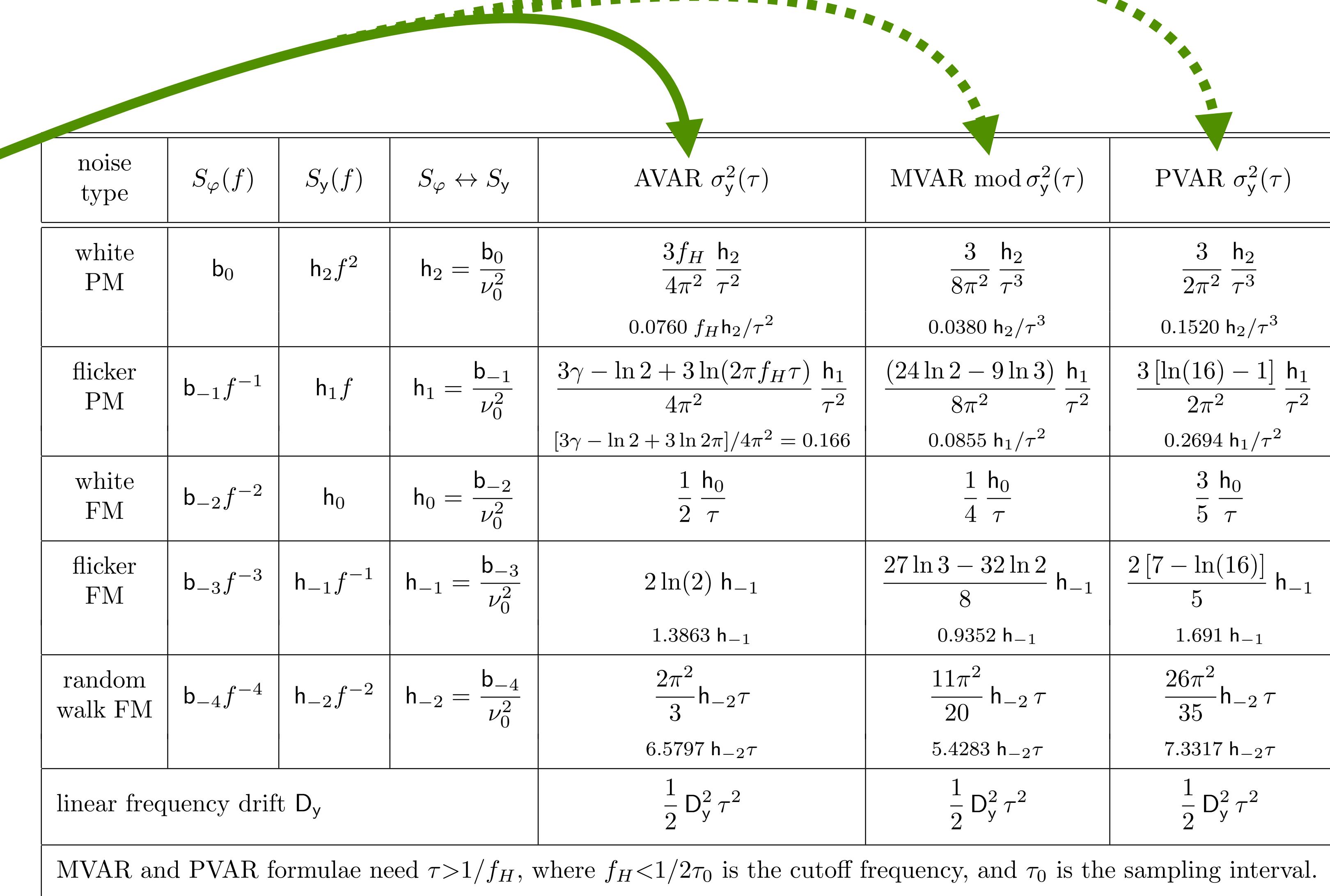


From $S_\varphi(f)$ to the Variances¹²

12



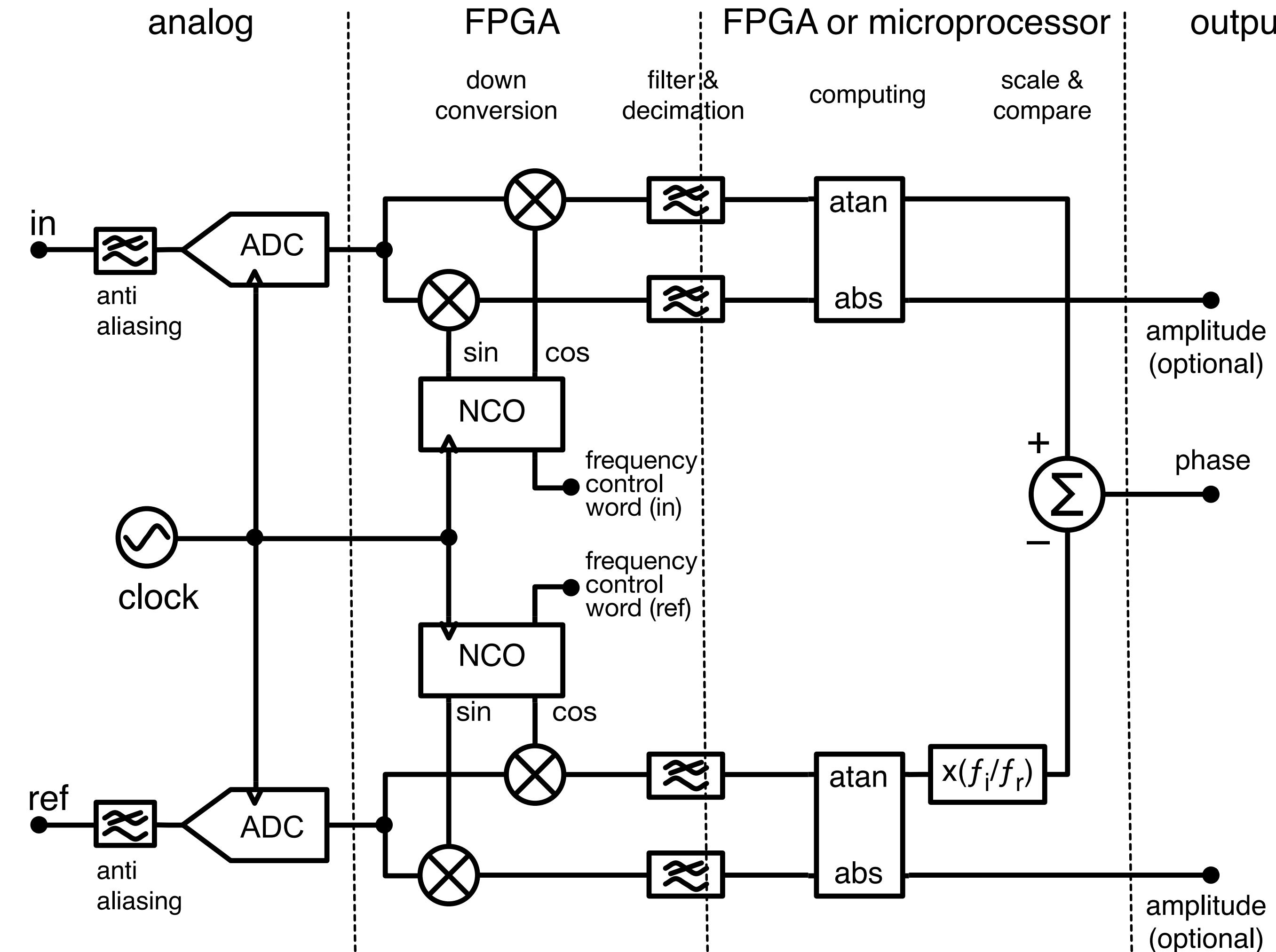
You may like the
Enrico's Noise Chart
on <http://rubiola.org>



The Measurement of Phase Noise

Direct Digitization

Add cross-spectrum for lower noise



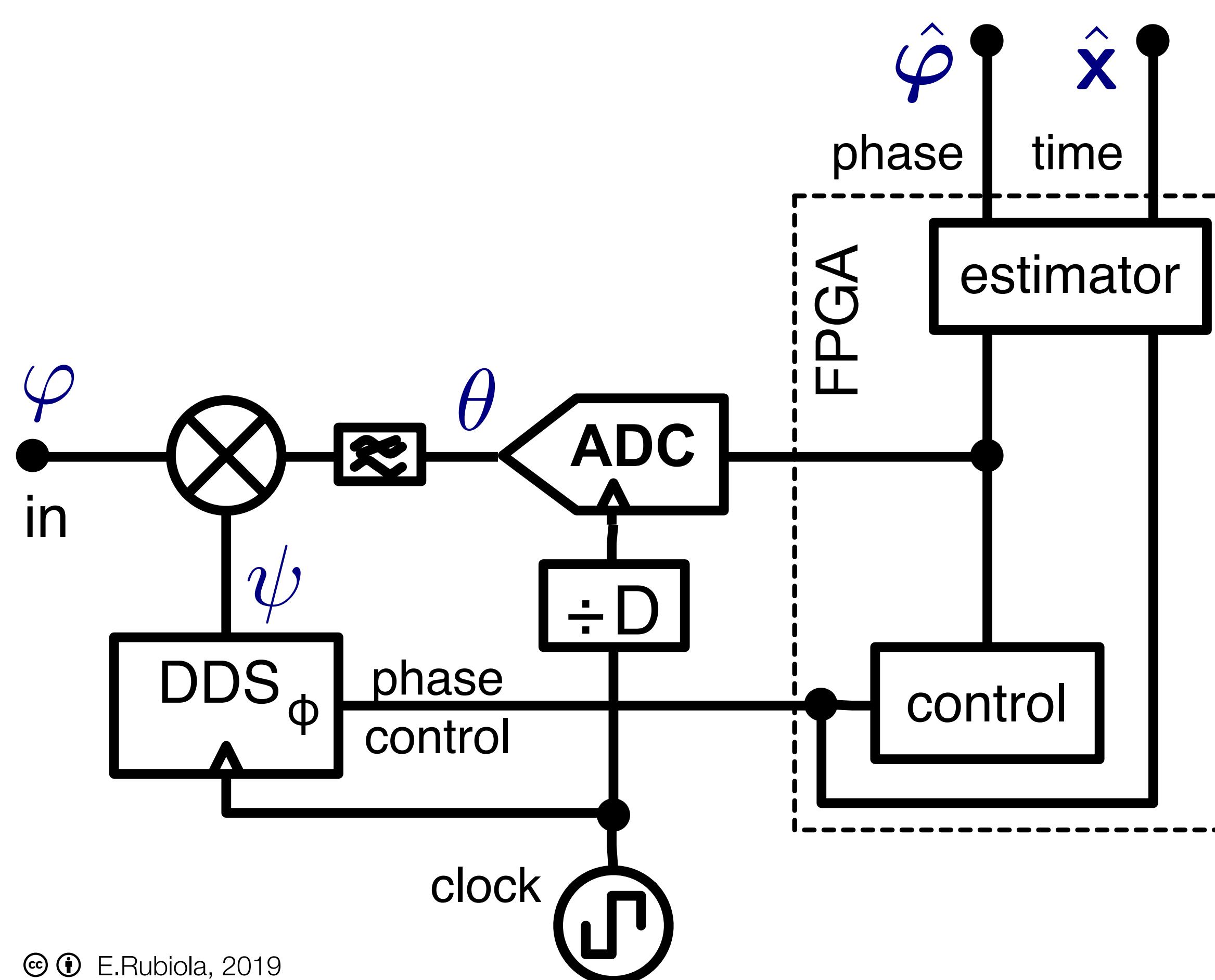
Outline

- Range 0...0.5 GHz w/o down converter
- High ADC's white and flicker noise,
 $b_0 \approx -160 \text{ dBrad}^2/\text{Hz}$
 $b_{-1} \approx -110 \text{ dBrad}^2$
- Arbitrary frequencies, $f_{\text{in}} \neq f_{\text{ref}}$ allowed
- Unwrapped phase
- Trace/plot time $x(t)$ and time error $x(t)$
- Allan(-like) variance(s)

Commercial products

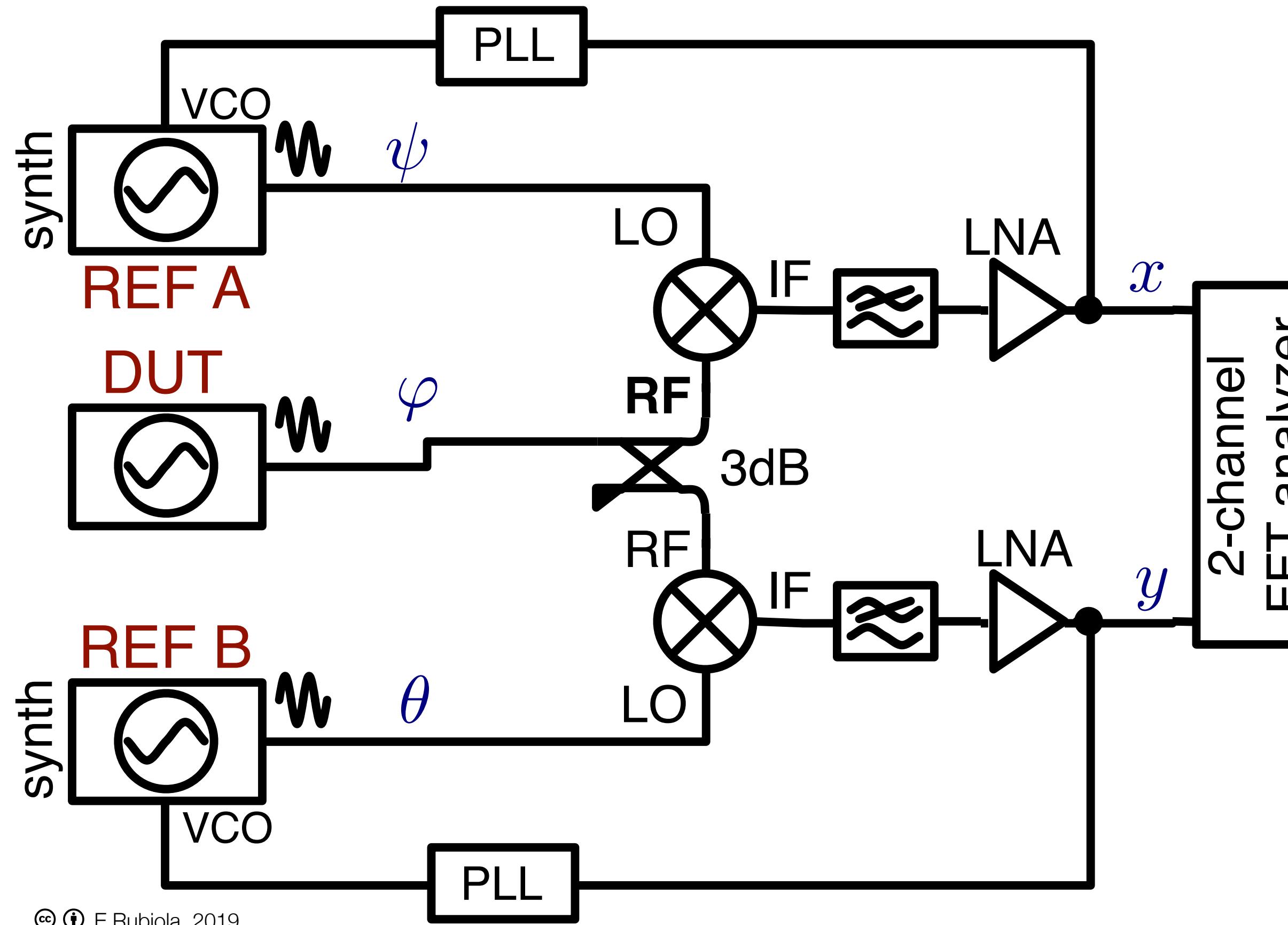
- Microsemi 3120A, 5120A (5125A → ?)
- Jackson Labs PhaseStation 53100A
- Rohde Schwarz FSWP (8/26/40 GHz,
no time and AVAR capability)

Tracking DDS (TDDS)



- DACs and DDSs have lower noise than ADCs
- The mixer noise is negligible
- DDS Control Word —> slow estimate of φ
- Combine Control Word ψ and the error θ provides fast estimate of φ
- Unwrapped phase gives $x(t)$ vs the clock
 - Full access to 2-sample variances
- Originally intended for time-domain measurements
- Single channel $\sigma_y = 1.4 \times 10^{-14}/\tau$
- Use two equal channels per input to reject the TDDS noise (cross spectrum or two-sample covariance)

The Traditional Scheme



From NIST, unable to find the original article

Commercial:
Anapico, BNC, Holzworth, Keysight, Noise XT,

Double Balanced Mixer

- Suitable to microwaves (40-60 GHz)
- Lowest background noise
 - White, $b_0 = -170 \dots -180 \text{ dBrad}^2/\text{Hz}$
 - Flicker, $b_{-1} \approx -120 \text{ dBrad}^2$ (μwave)
 $b_{-1} = -130 \dots -140 \text{ dBrad}^2$ (RF)

But

- Narrow phase range, $\pm 0.1 \text{ rad} (\pm 6^\circ)$
- No phase unwrapping
- Low $\varphi \rightarrow v$ gain (0.1...0.5 V/rad)
- High sensitivity to 50-60 Hz B fields because of low output voltage
- ...and other flaws

Noise Rejection Law

Cross spectrum

$$S_{yx}(f) = \frac{2}{T} Y(f) X^*(f)$$

All the signal goes in $\text{Re}\{S_{yx}\}$

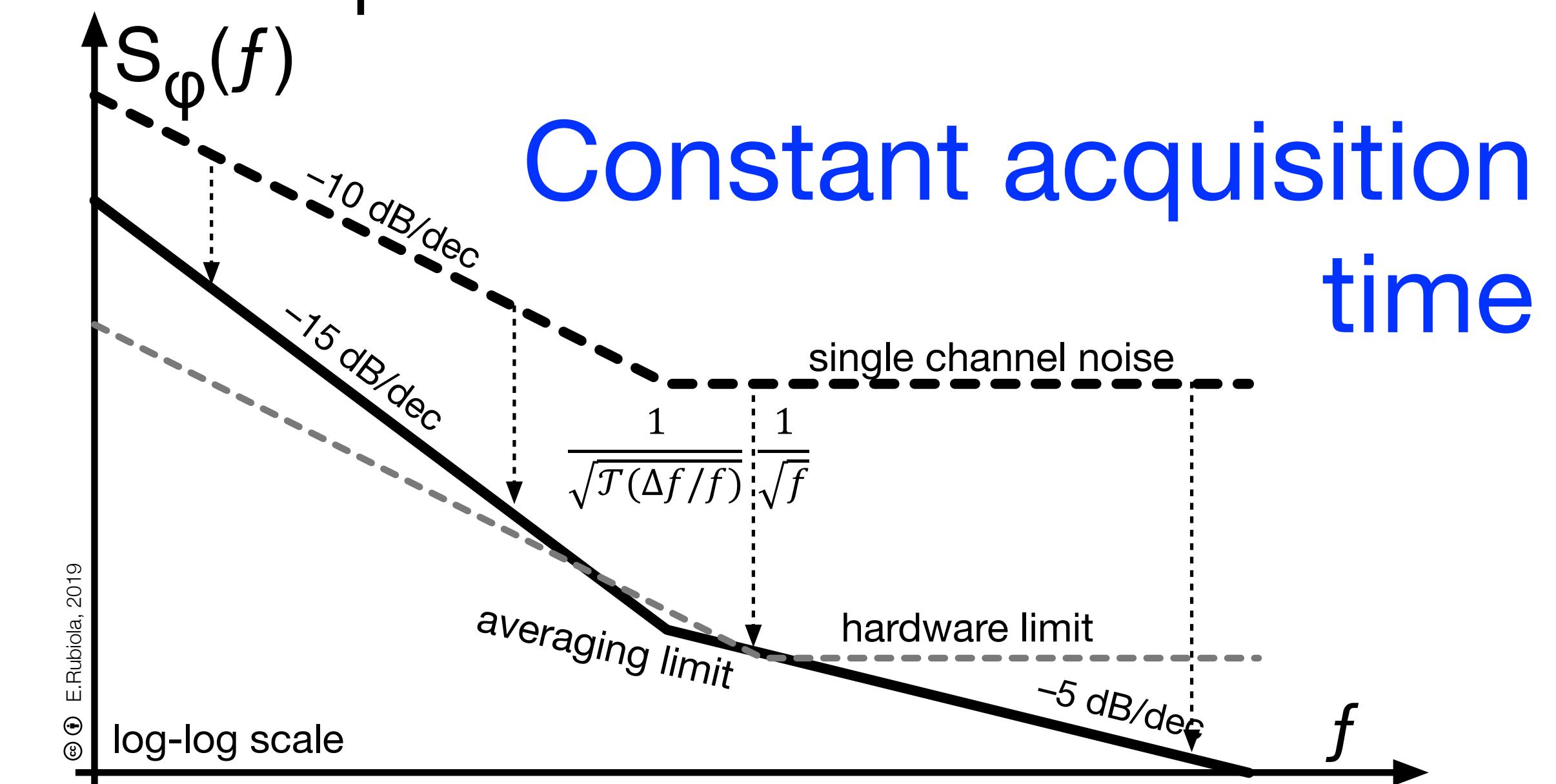
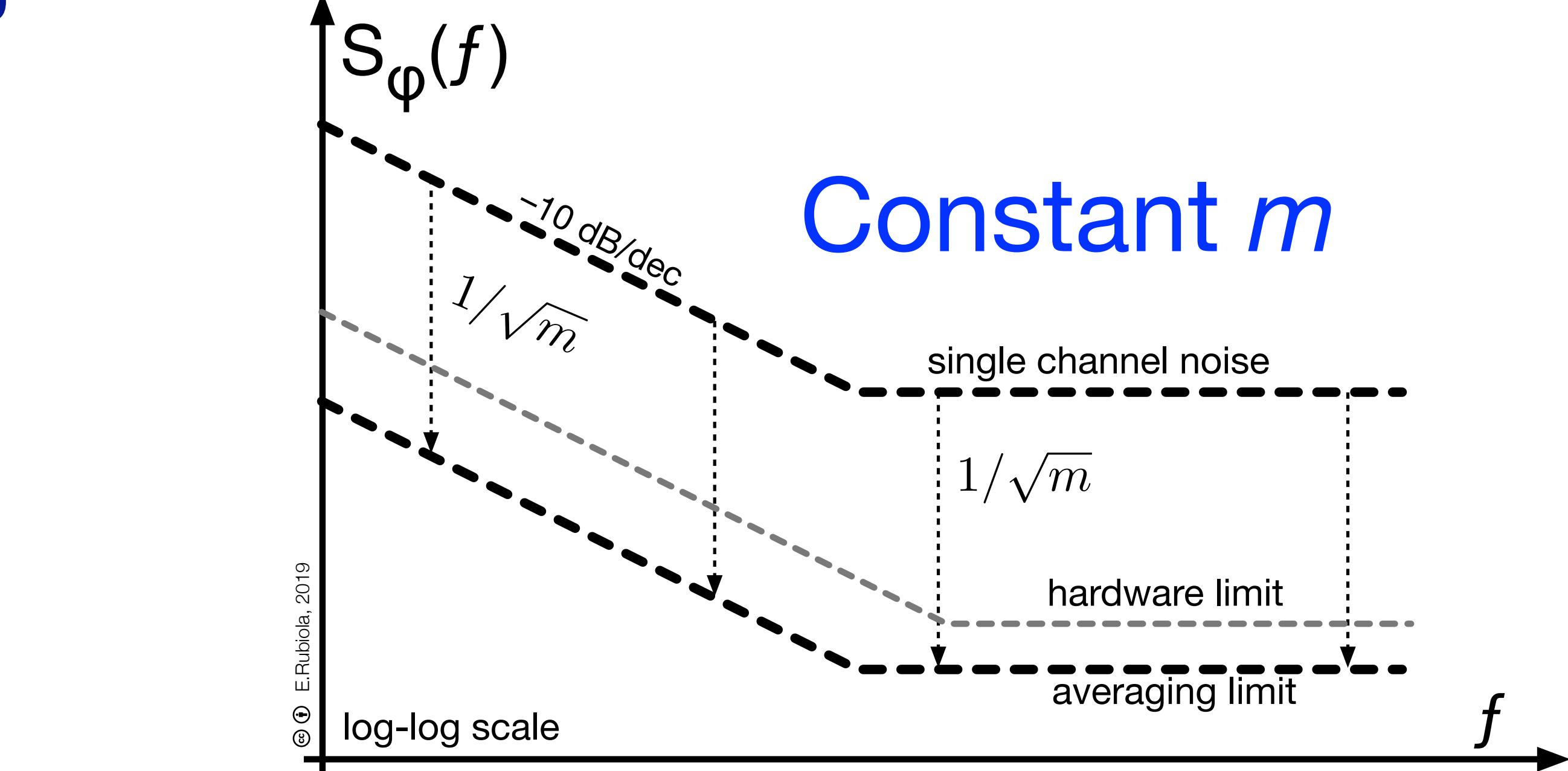
$$\Re \left\{ \left\langle S_{yx}(f) \right\rangle_m \right\} = S_\phi(f) + O(1/m)$$

$\text{Im}\{S_{yx}\}$ contains only background noise

$$\Im \left\{ S_{yx}(f) \right\} = O(1/m)$$

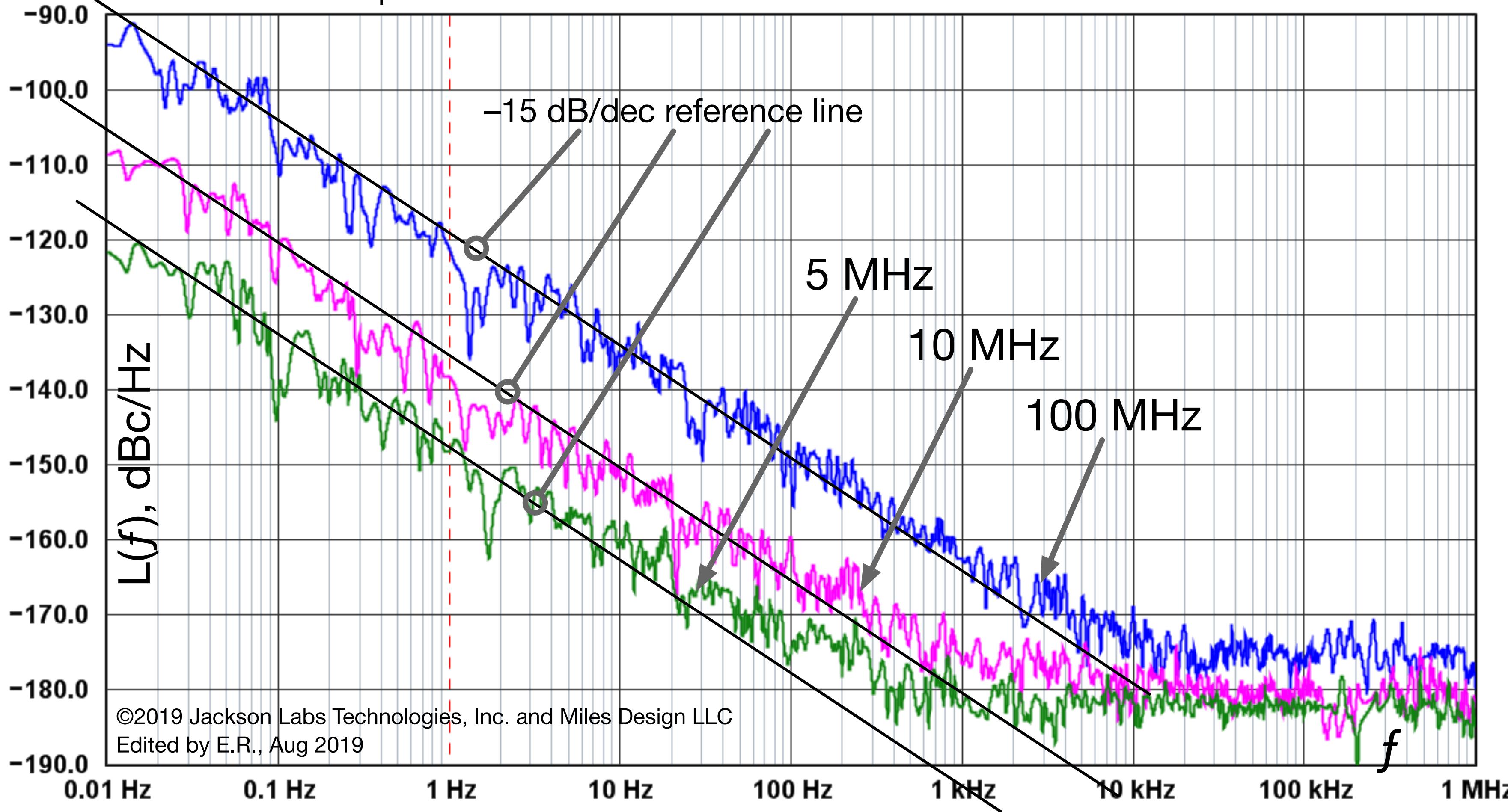
Manufacturers use $\left| \left\langle S_{yx}(f) \right\rangle_m \right|$

E. Rubiola, F. VERNOTTE, The cross-spectrum experimental method, Feb 2010, arXiv:1003.0113 [physics.ins-det].



Example

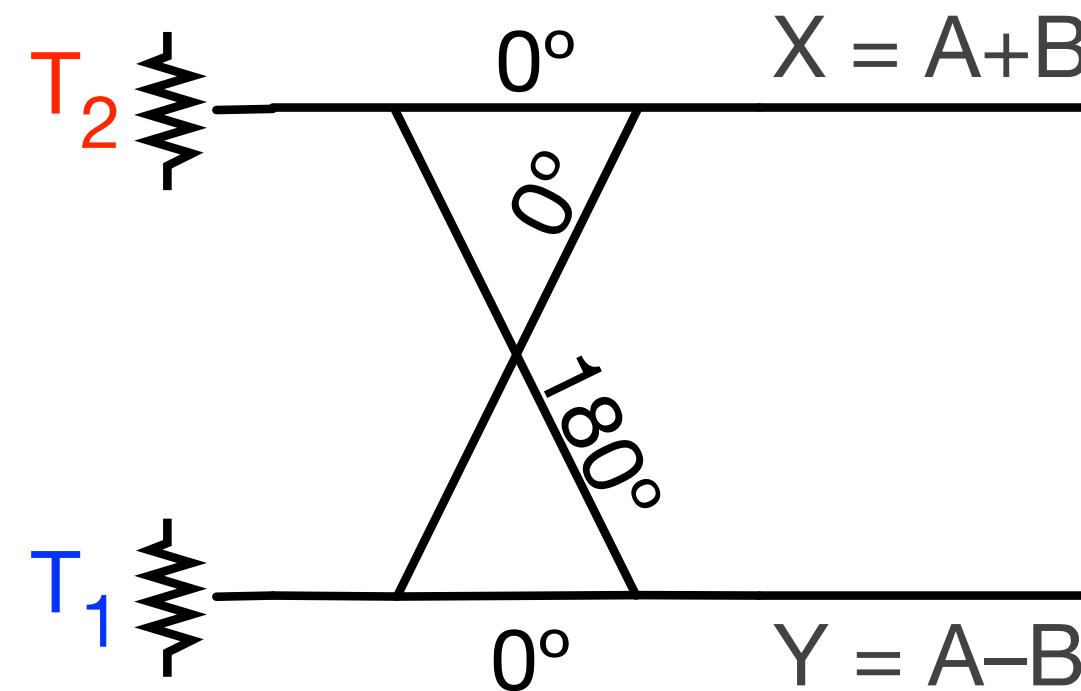
Background PM Noise of the PhaseStation 53100A
Input and reference connected to the same oscillator



Trace	Input Freq	Input Amplitude	dBc/Hz at 1 Hz	Elapsed	Instrument
100 MHz residual floor	100.0 MHz	11 dBm	-121.1	58m 49s	PhaseStation 53100A
10 MHz residual floor	10.0 MHz	12 dBm	-138.2	33m 5s	PhaseStation 53100A
5 MHz residual floor	5.0 MHz	12 dBm	-148.2	8h	PhaseStation 53100A

Flaws of the Cross Spectrum

Dark-Port Temperature

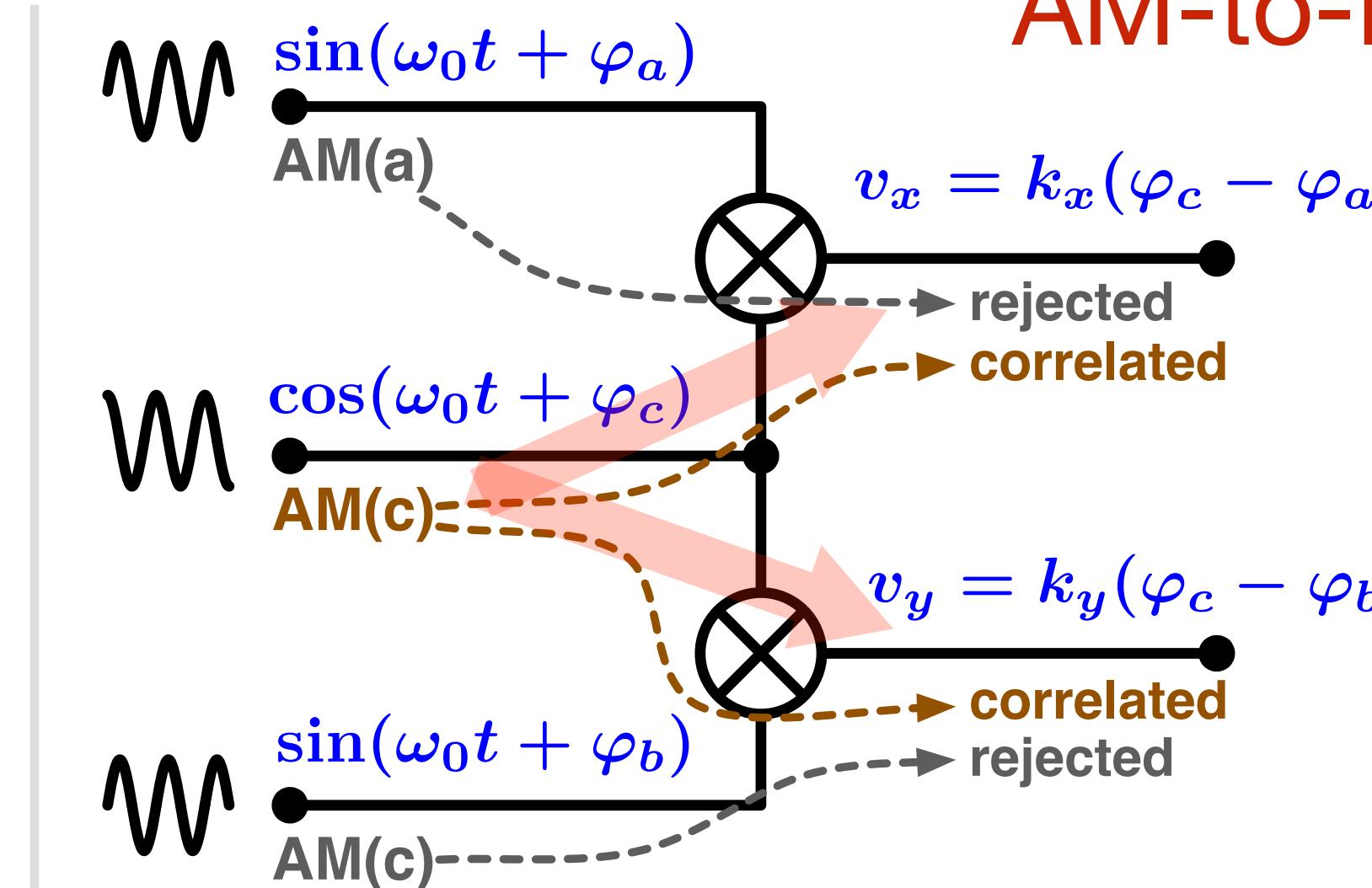


$$S_{yx} = \frac{1}{2}k(T_2 - T_1)$$

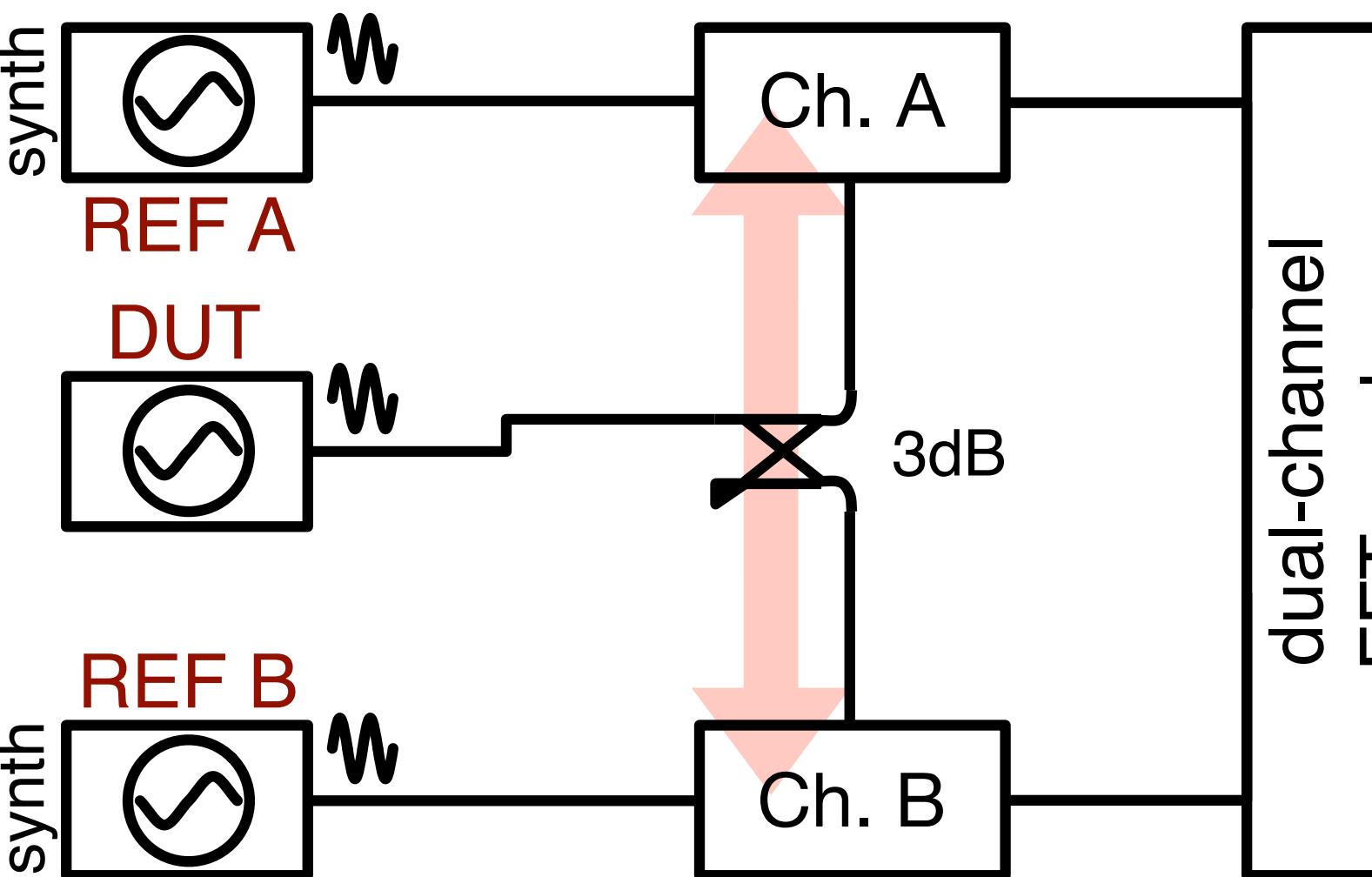
Systematic error

Y. Gruson & al, IEEE T UFFC 64(3) p.634-641, Mar 2017

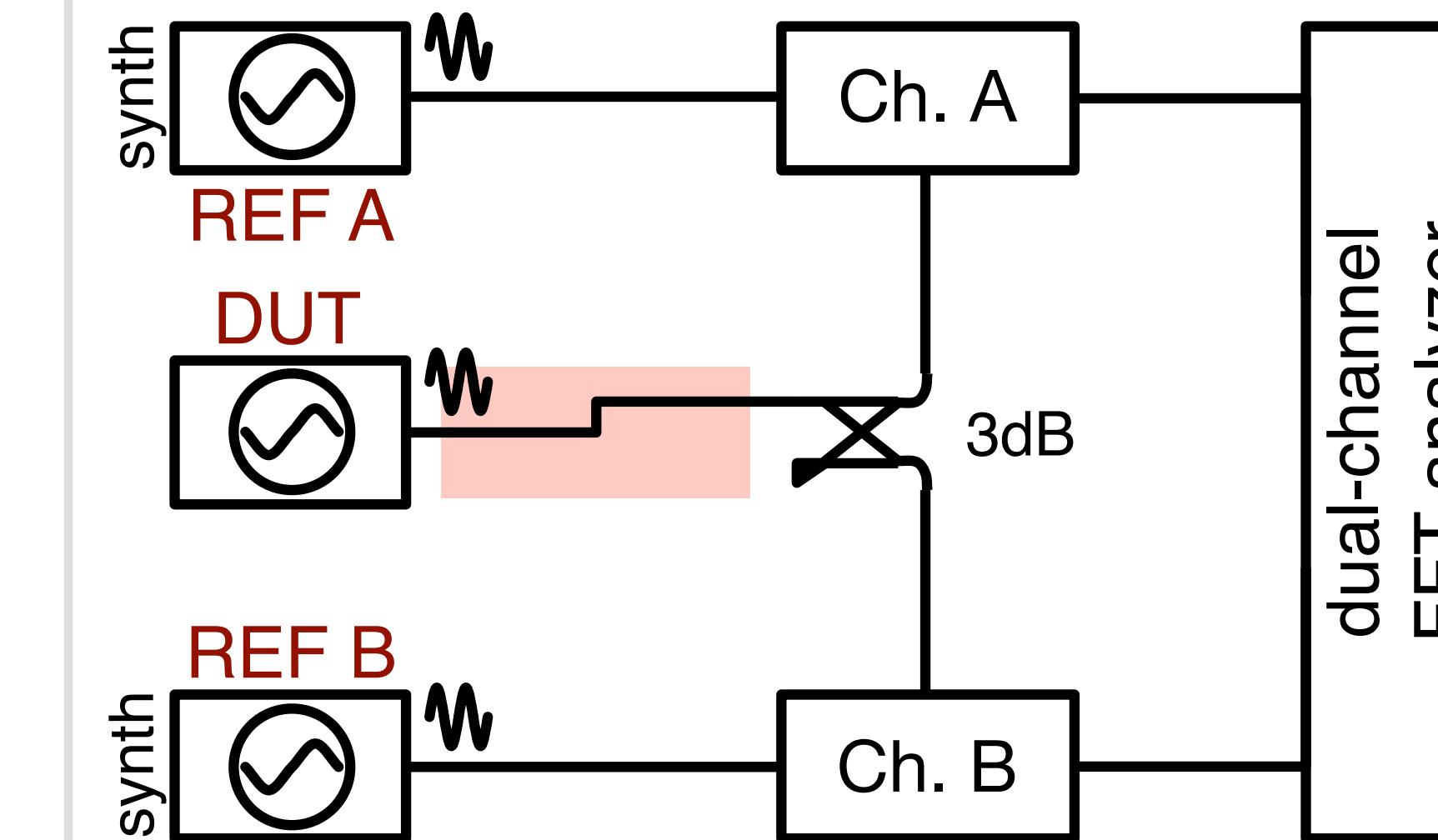
AM-to-DC Conversion



No way to
divide the effect
of AM from PM



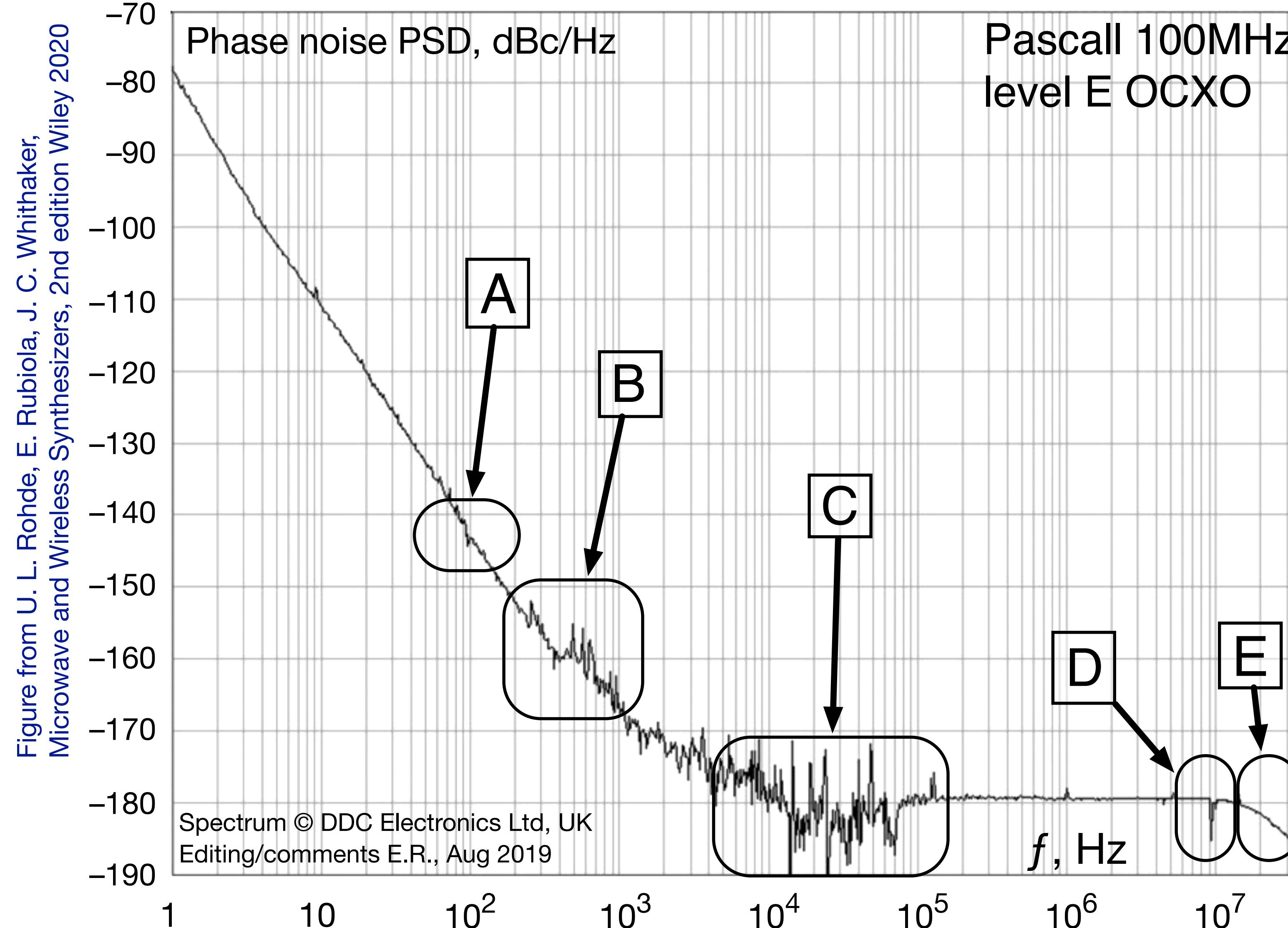
Crosstalk
has sign!!!



Impedance
mismatch

Erratic
behavior
reported

Example of Odd Spectrum

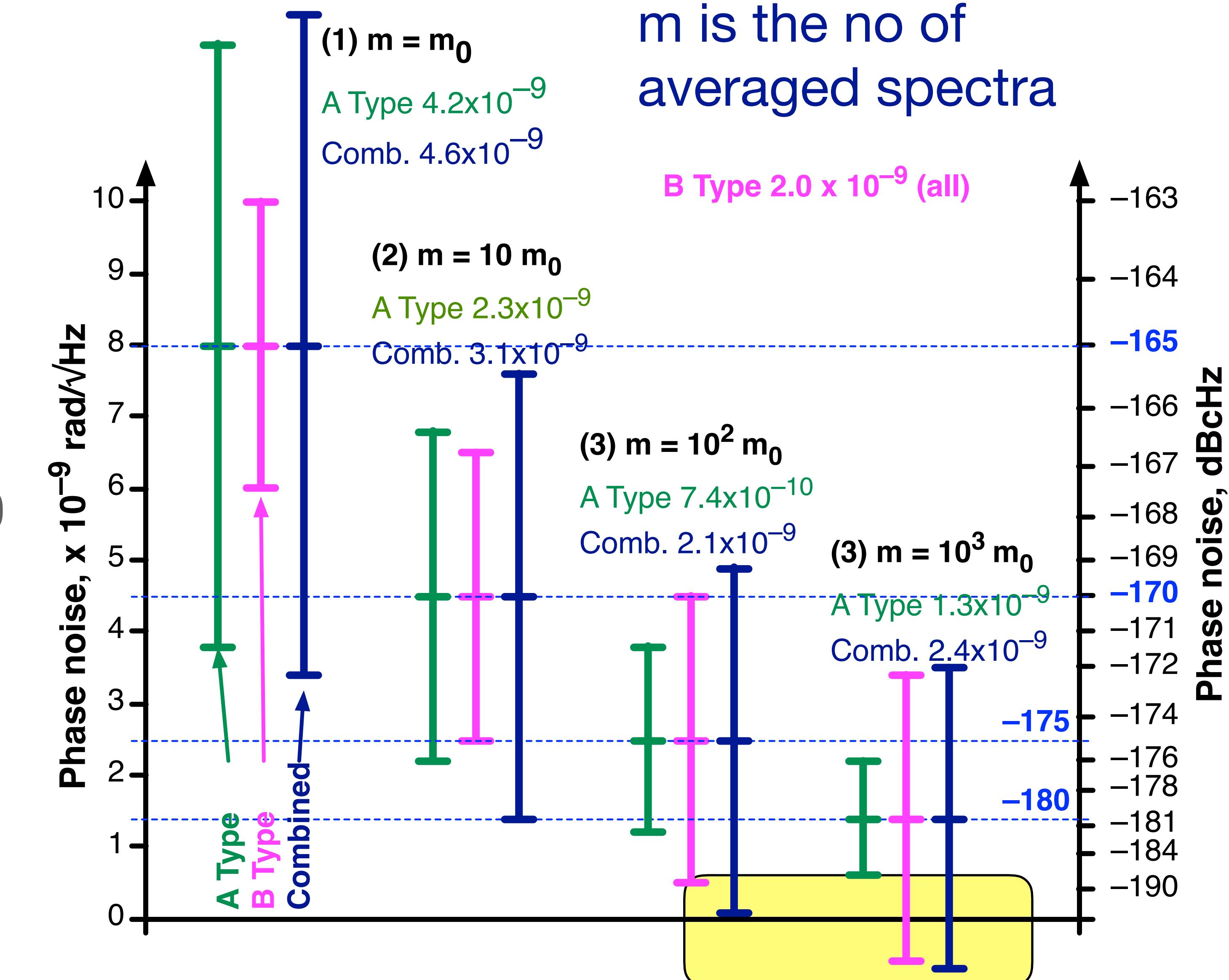


Type-A, Type B, and Null Uncertainty

BIPM GUM

- A-type (noise-like) uncertainty
- B-type (system) uncertainty
- Combined $U^2 = A^2 + B^2$
- “Regular” case $S \rightarrow S_0 \pm U$
- Zero uncertainty, applies to $S > 0$
When $S_0 \pm U$ hits 0,
the outcome is 0
with zero-uncertainty of U

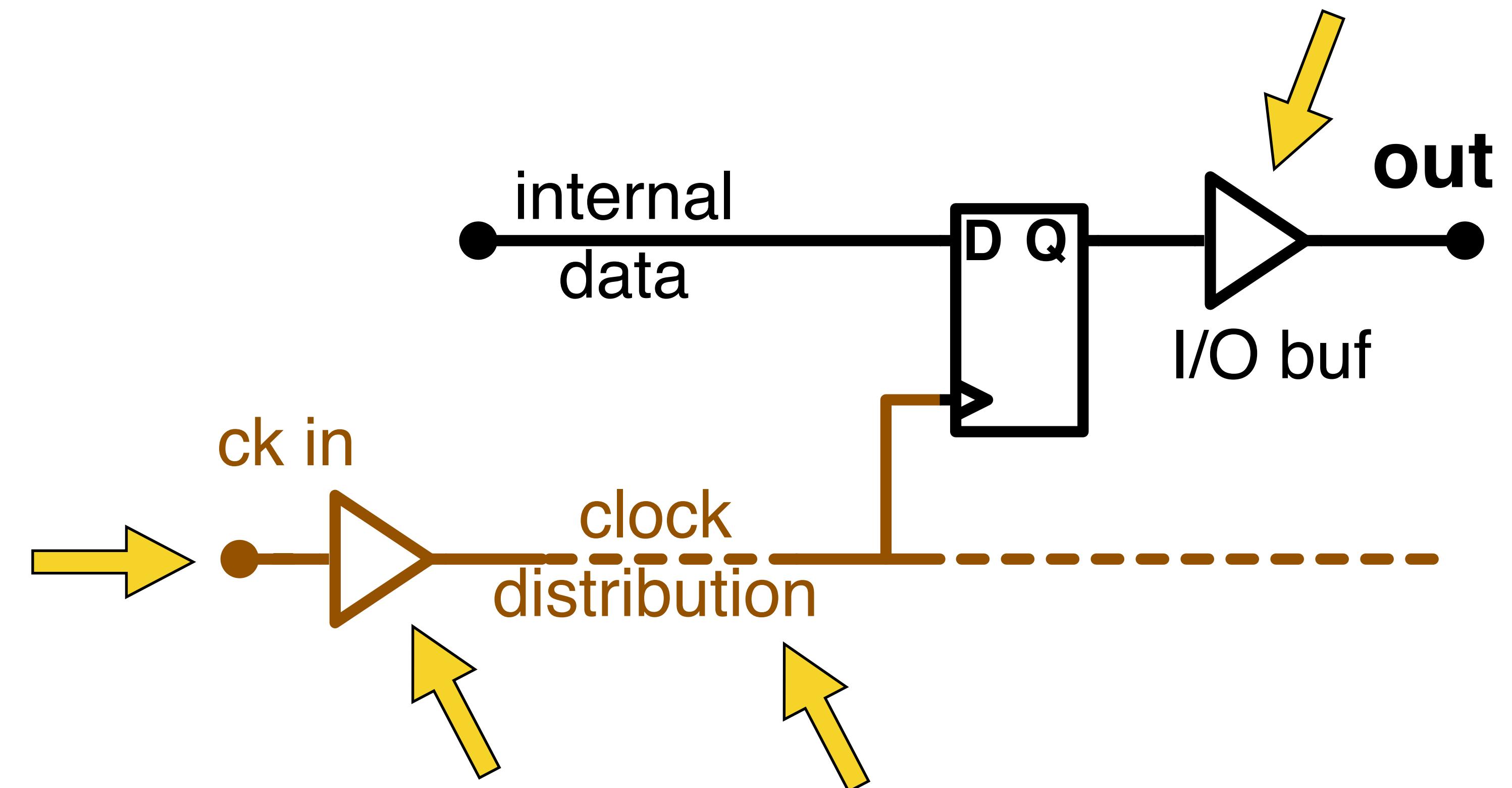
Pushing the instruments to the limit
takes deep understanding of the system and of metrology



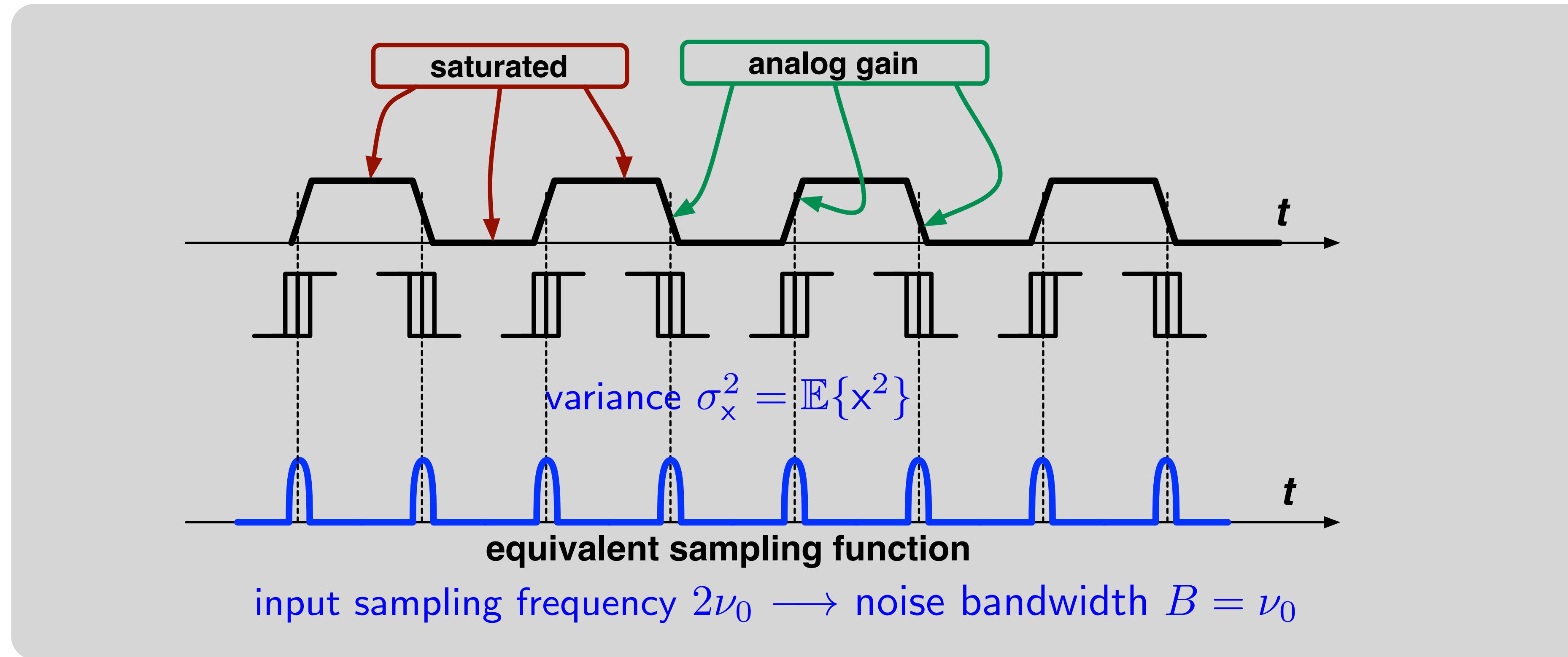
PM Noise in Digital Circuits

Output Time Fluctuation

- Output can be synchronized to the clock
- Time fluctuation cannot be smaller than
 - External clock signal
 - Clock input stage
 - Clock distribution
 - Output stage



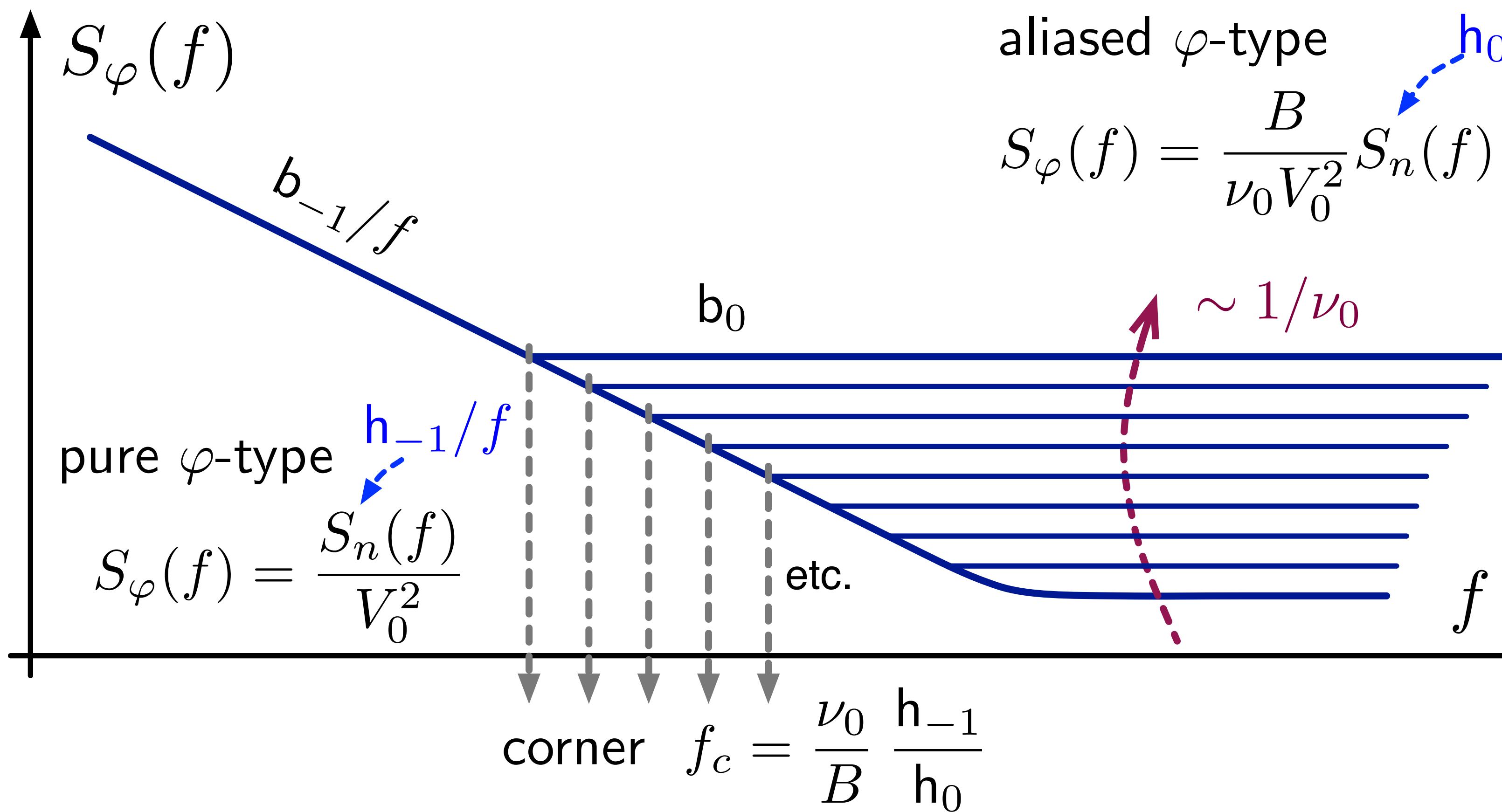
Phase Noise Sampling



- Sampling occurs at the edges
 - (in some cases, only at rising or falling edges)
- Square wave signals need analog bandwidth at least $3 V_{max} \dots 4 V_{max}$
- Aliasing is around the corner

Phase-Type (φ -type) PM Noise

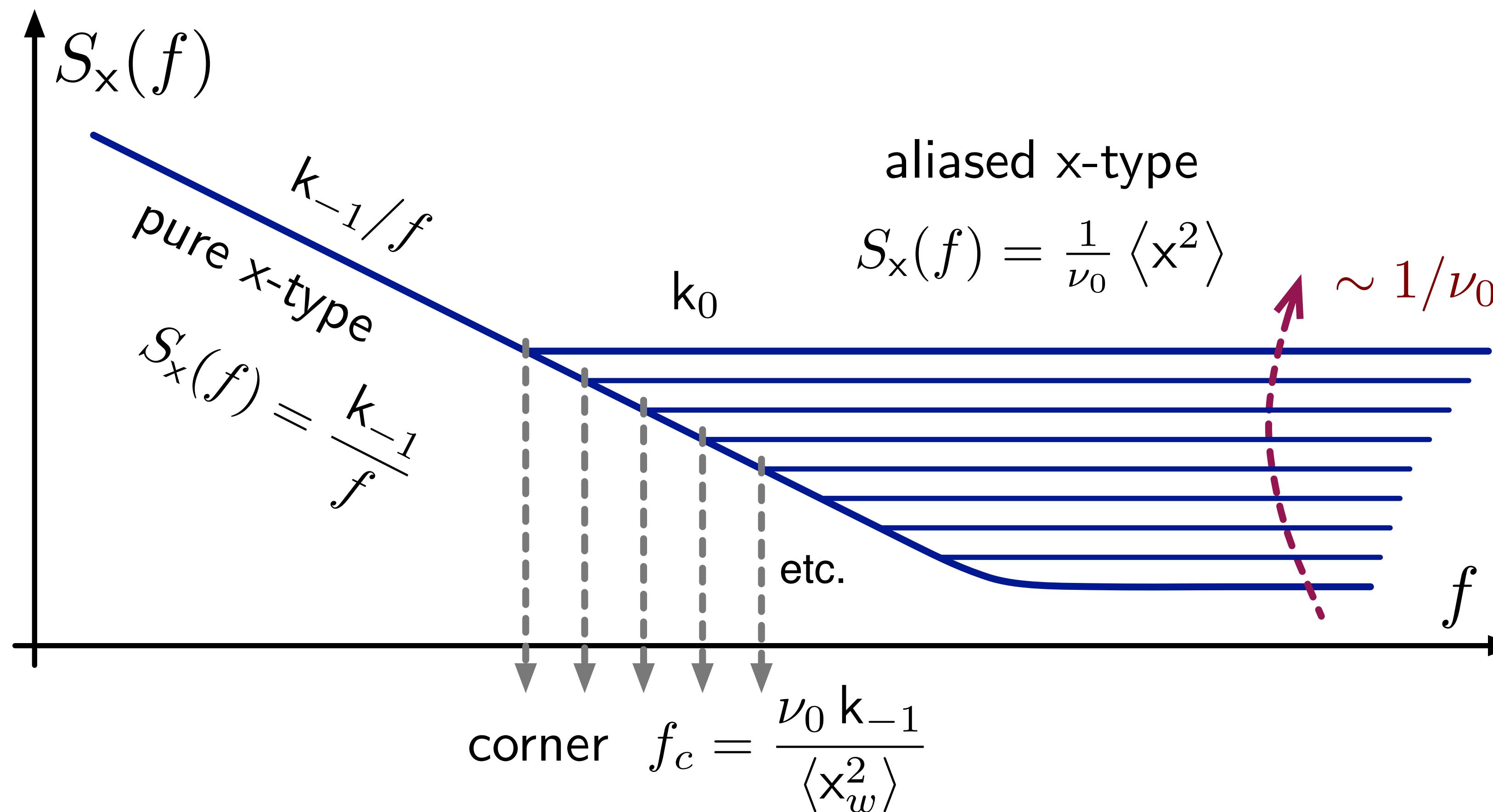
Aliasing strikes hard on white noise, yet little/not on flicker



Polynomial law $S_n(f) = \sum h_i f^i$ [do not mistake with $S_y(f)$]

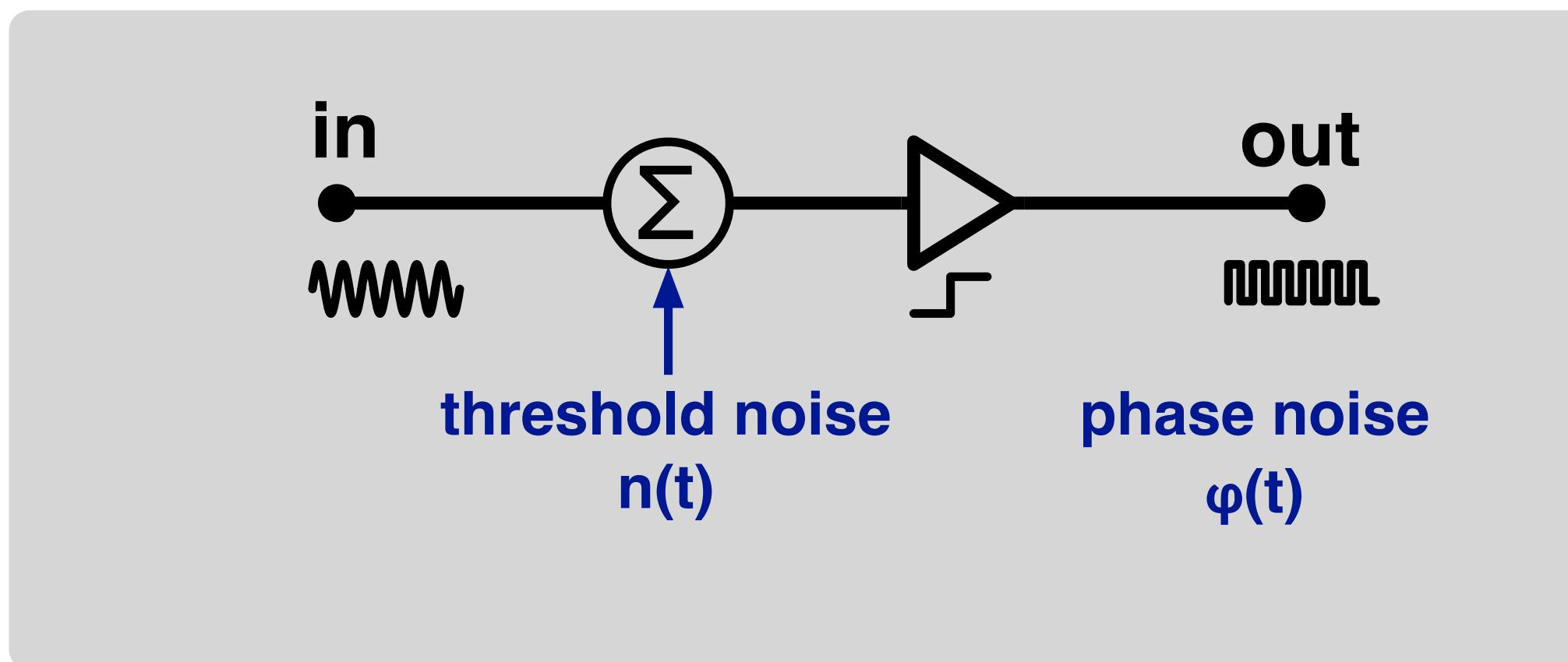
Time-Type (x-type) Fluctuation

Aliasing strikes hard on white noise, yet little/not on flicker



$$\text{Polynomial law } S_x(f) = \sum k_i f^i$$

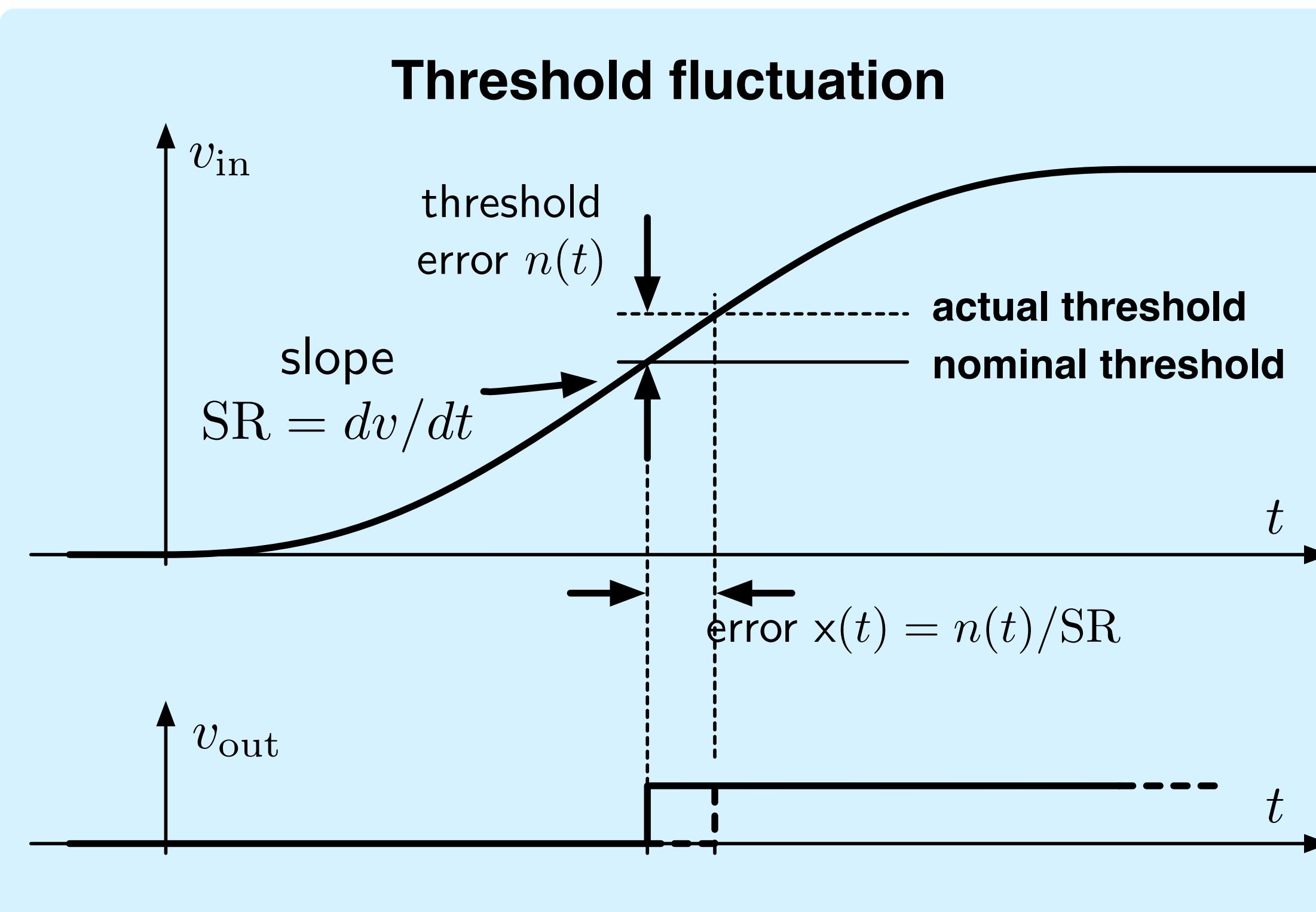
Phase Noise in the Input Stage



Sinusoid of peak amplitude V_0
results in phase-type noise

$$S_\varphi(f) = \frac{S_n(f)}{V_0^2}$$

constant vs ν_0

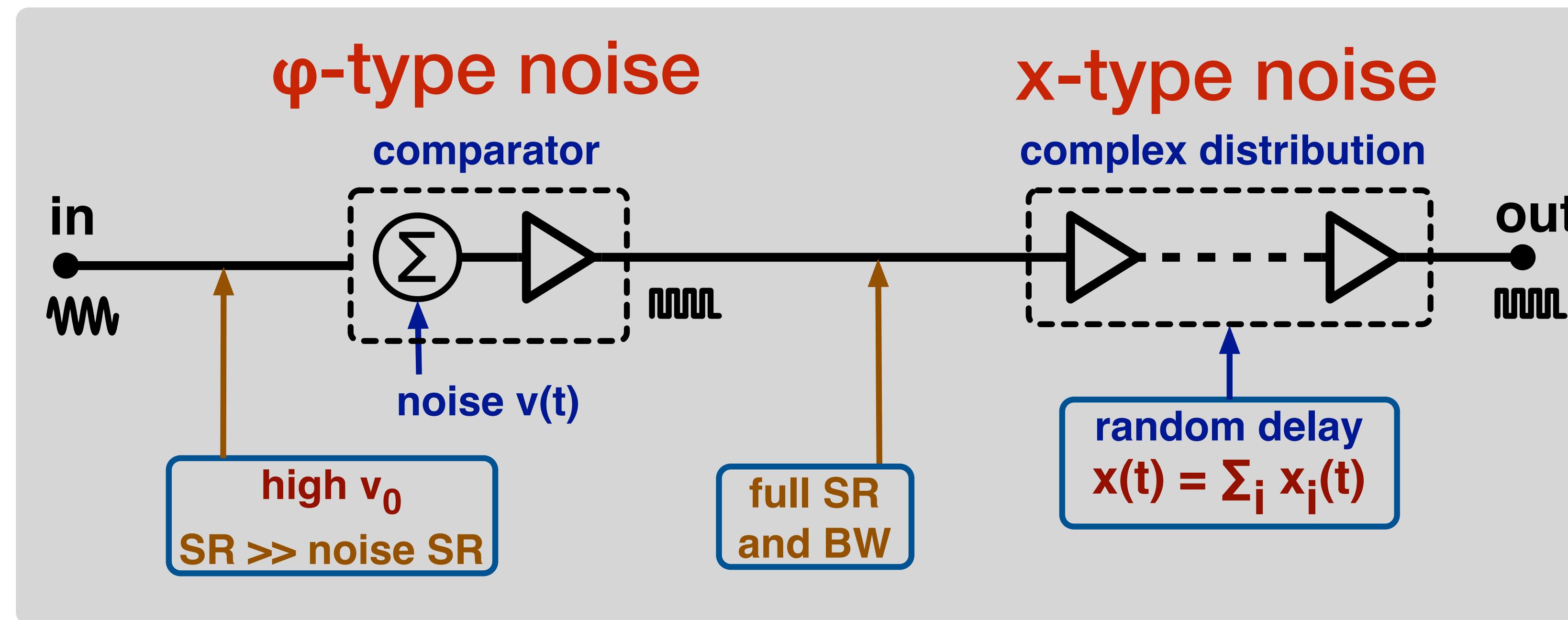


mechanism

$$x(t) = \frac{n(t)}{(SR)(t)}$$

$$\varphi(t) = \frac{2\pi\nu_0 n(t)}{(SR)(t)}$$

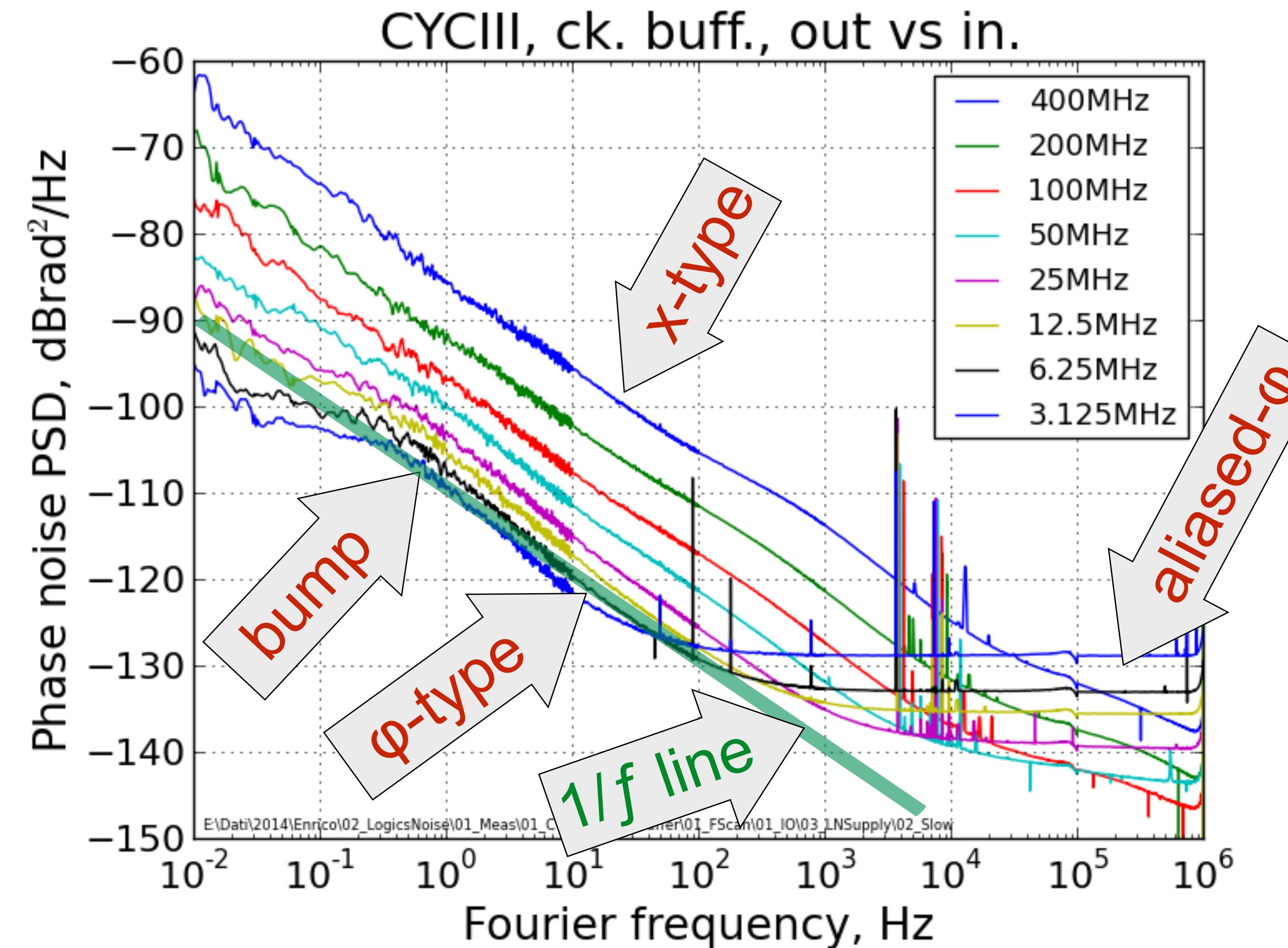
Full Noise Mechanism



- The φ -type noise noise may show up or not, depending on input noise and SR
- At the comparator out, the edges attain full SR and bandwidth of the technology
- Complex distribution → independent fluctuations add up

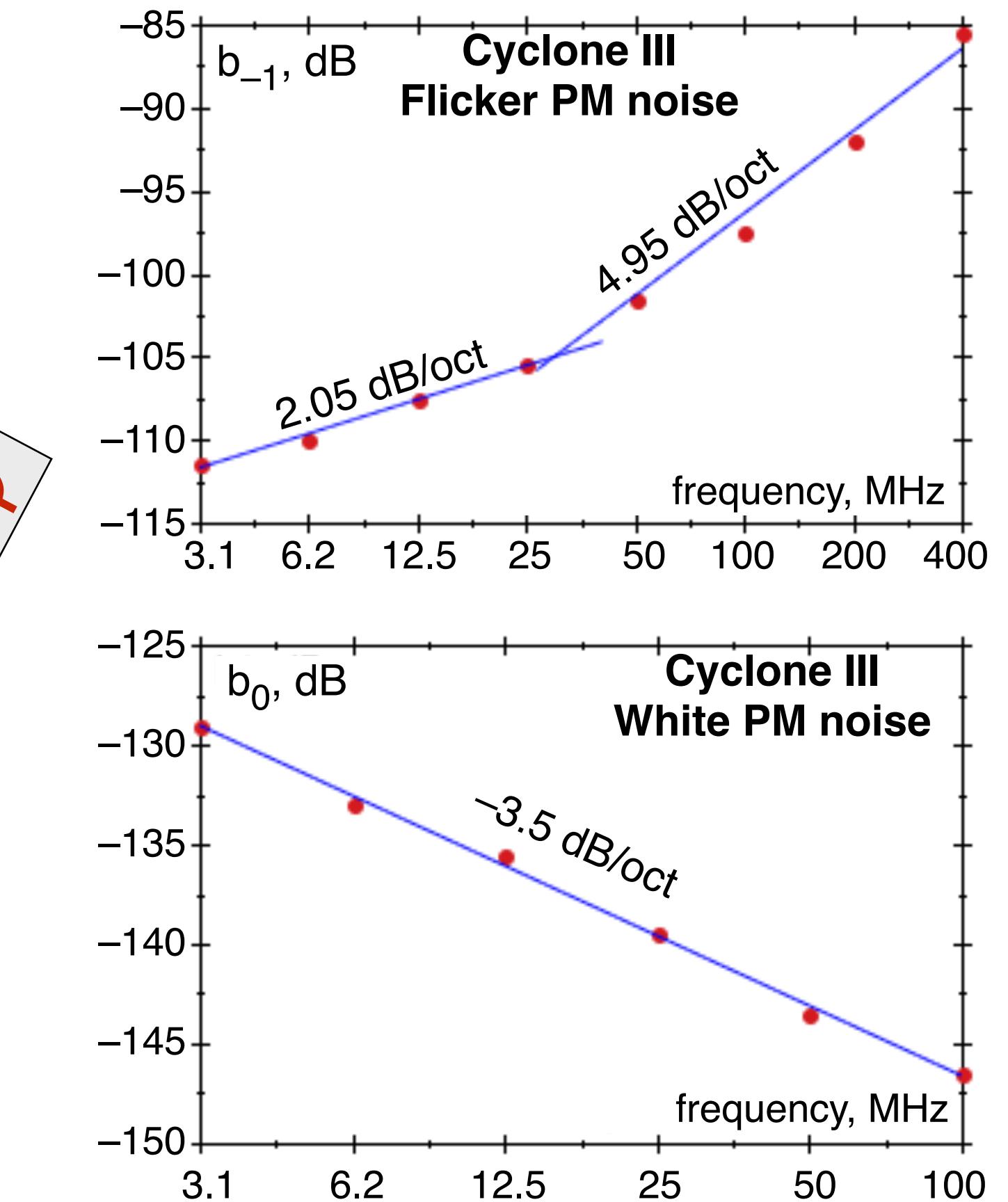
$$x(t) = \sum_i x_i(t) \quad \text{and} \quad \langle x^2(t) \rangle = \sum_i \langle x_i^2(t) \rangle$$

Cyclone III Clock Buffer



Flicker

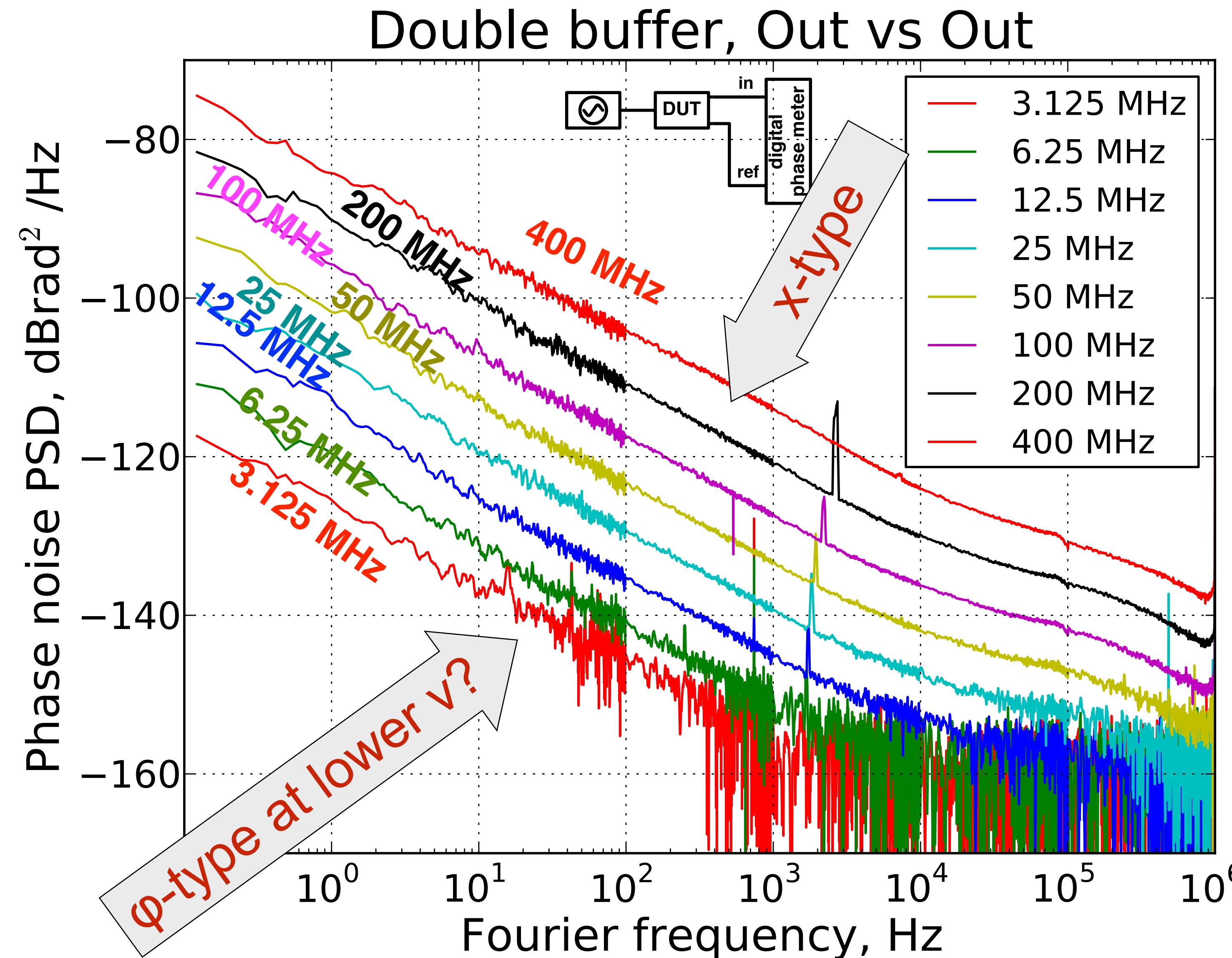
- High v_0 \rightarrow scales as v_0 (x-type)
- Low v_0 , \rightarrow to φ -type (bumps 0.1–10 Hz)



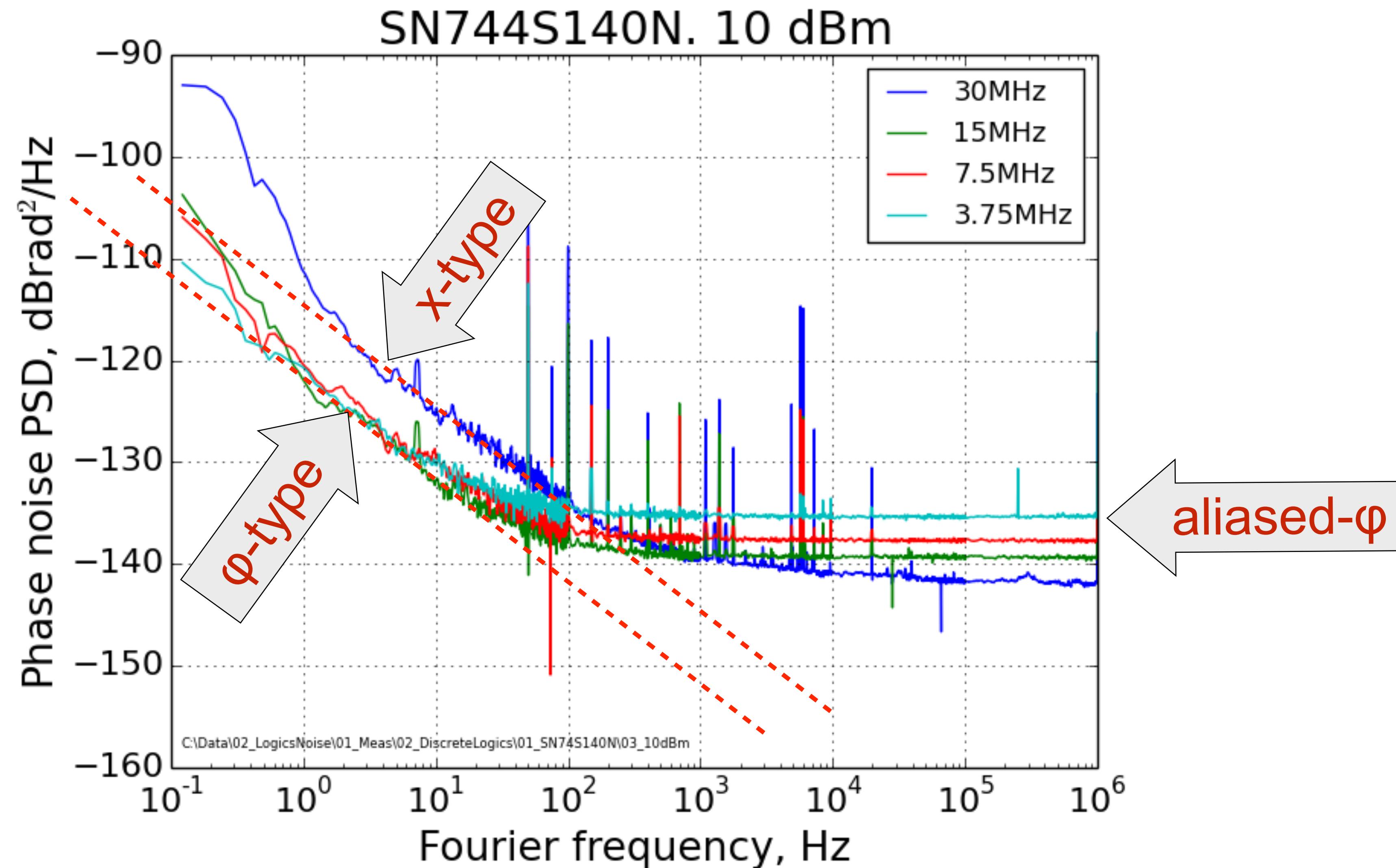
White

- Aliasing shows up at low v_0

Cyclone III Output Buffer



74S140 – Old TTL 50 Ω Driver



Additional Facts

Volume Law

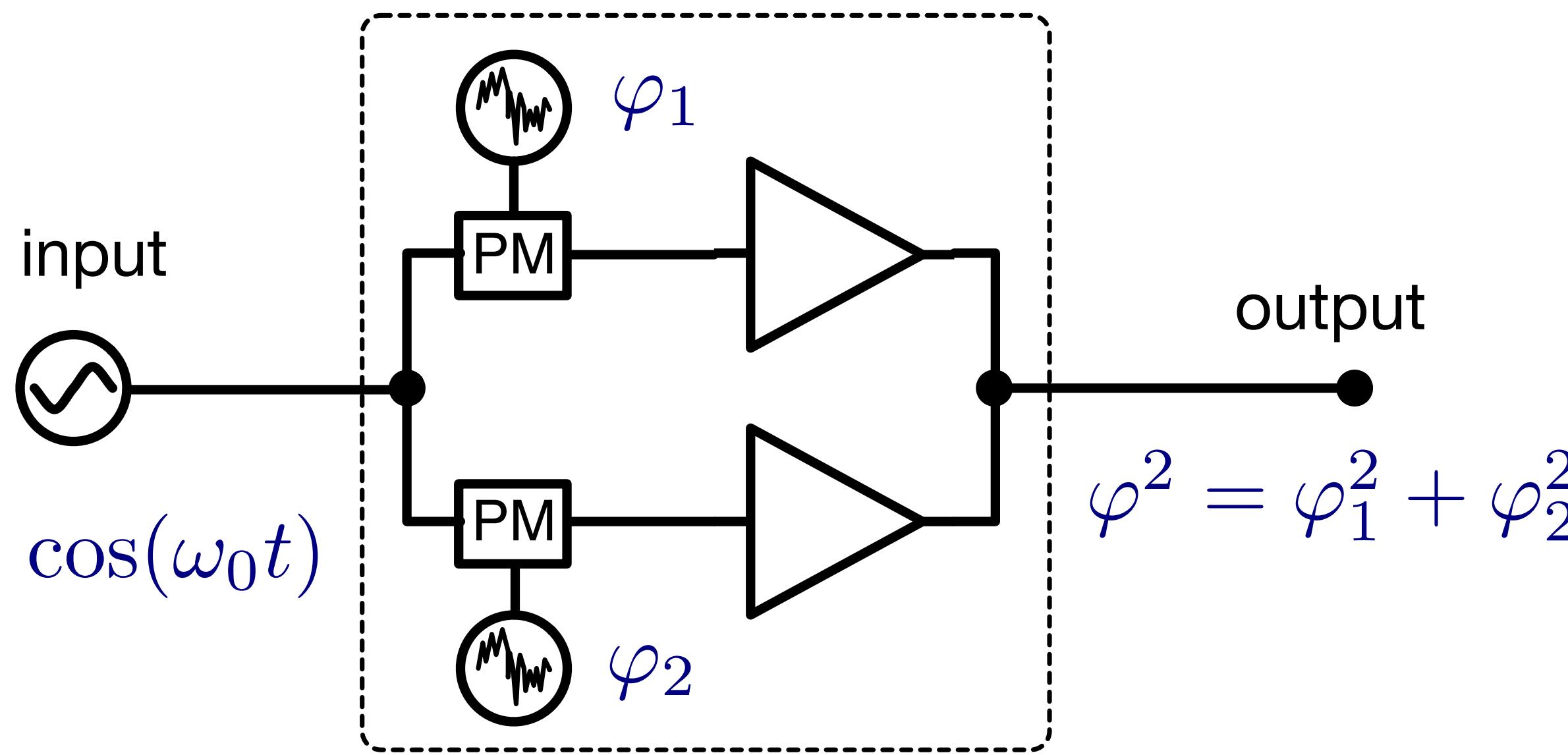
Input Chatter

Internal PLL

Thermal Effects

The Volume Law

Experiment



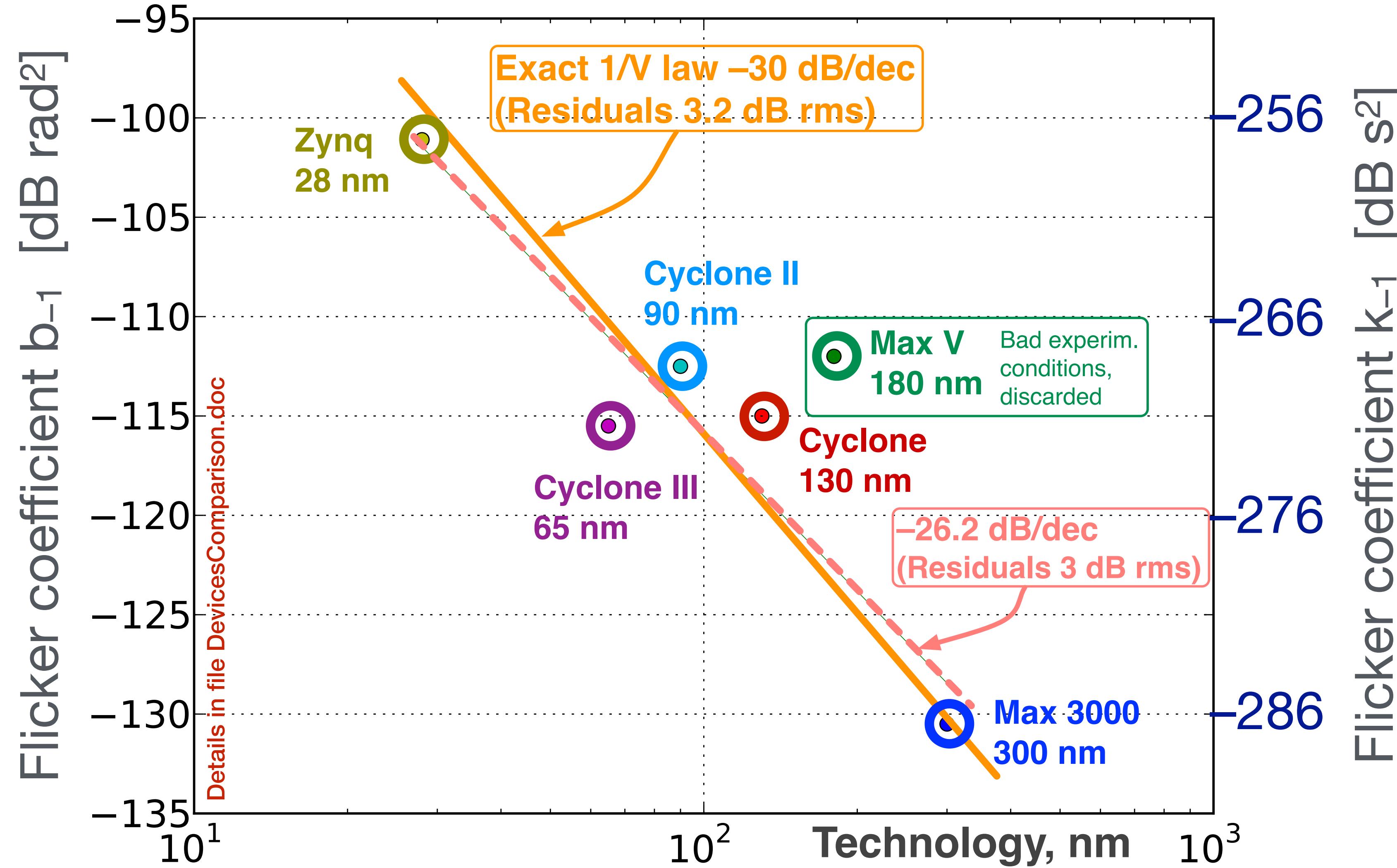
- The $1/f$ coefficient b_{-1} is independent of power
- The flicker of a branch does not increase at $P/2$
- At the output,
 - the carrier adds up coherently
 - the phase noise adds up statistically
- With m branches, the $1/f$ PM noise is reduced by $1/m$
- White noise cannot be reduced in this way

Gedankenexperiment

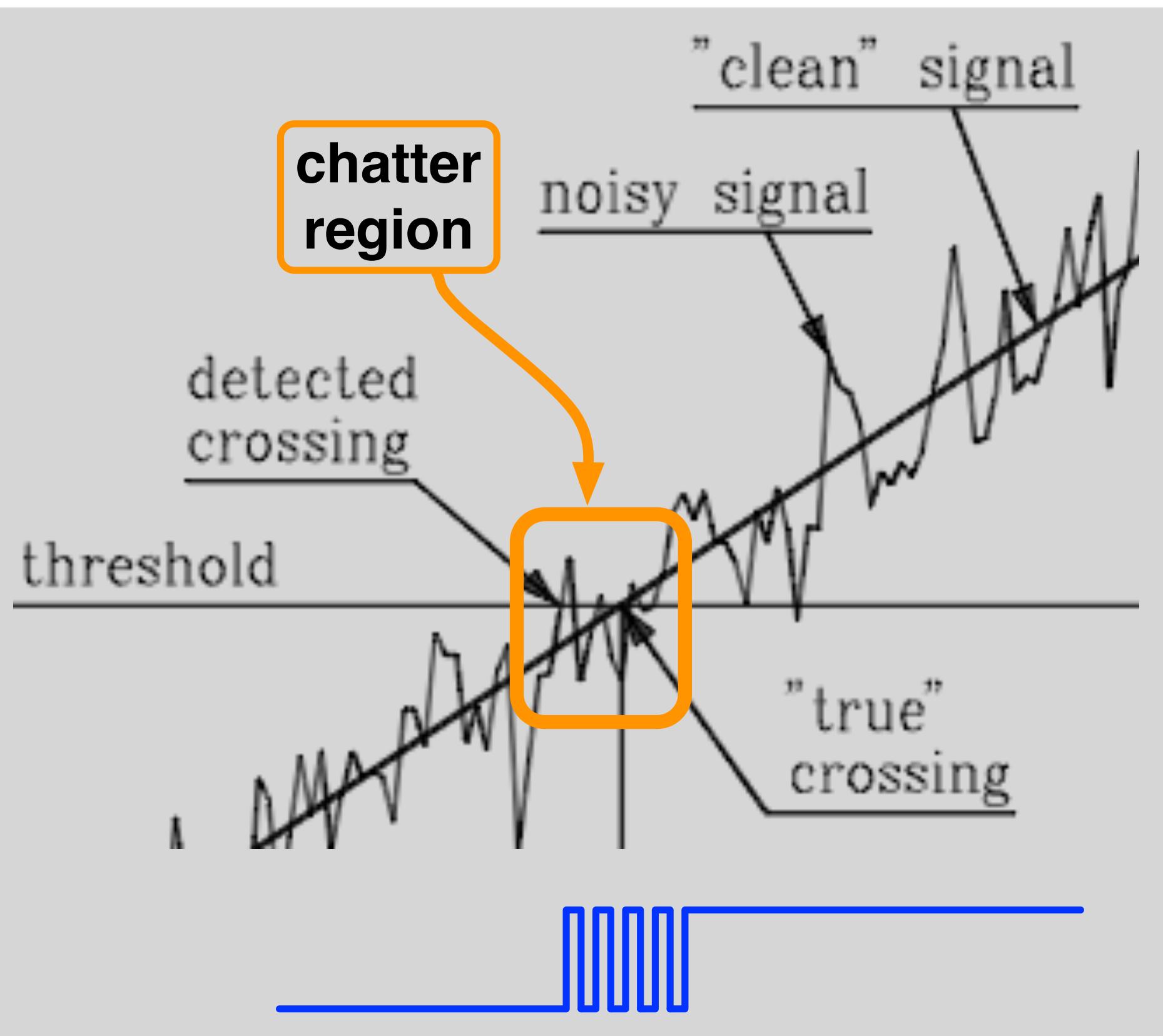
- Flicker is of microscopic origin because it has Gaussian PDF
- Join the m branches into a compound
- $1/f$ noise is proportional to $1/V$, the volume of the active region

The Volume Law!

All devices used as $\div 10 \Lambda$ divider at 100 MHz input
 (30 MHz with Cyclone and Cyclone II, and results are scaled up as x-type noise)
 The Λ divider reduces aliasing (white), thus makes 1/f noise more visible



Input Chatter



With high-speed devices, chatter can occur at rather high frequencies

Chatter occurs when the RMS Slew Rate of noise exceeds the slew rate of the pure signal

Pure signal

$$v(t) = V_0 \cos(2\pi\nu_0 t)$$

$$\text{SR} = 2\pi\nu_0 V_0$$

Wide band noise

$$\begin{aligned} \langle \text{SR}^2 \rangle &= 4\pi^2 \int_0^B f^2 S_V(f) df \\ &= \frac{4\pi^2}{3} \sigma_V^2 B^2 \quad (\text{rms}) \end{aligned}$$

Chatter threshold

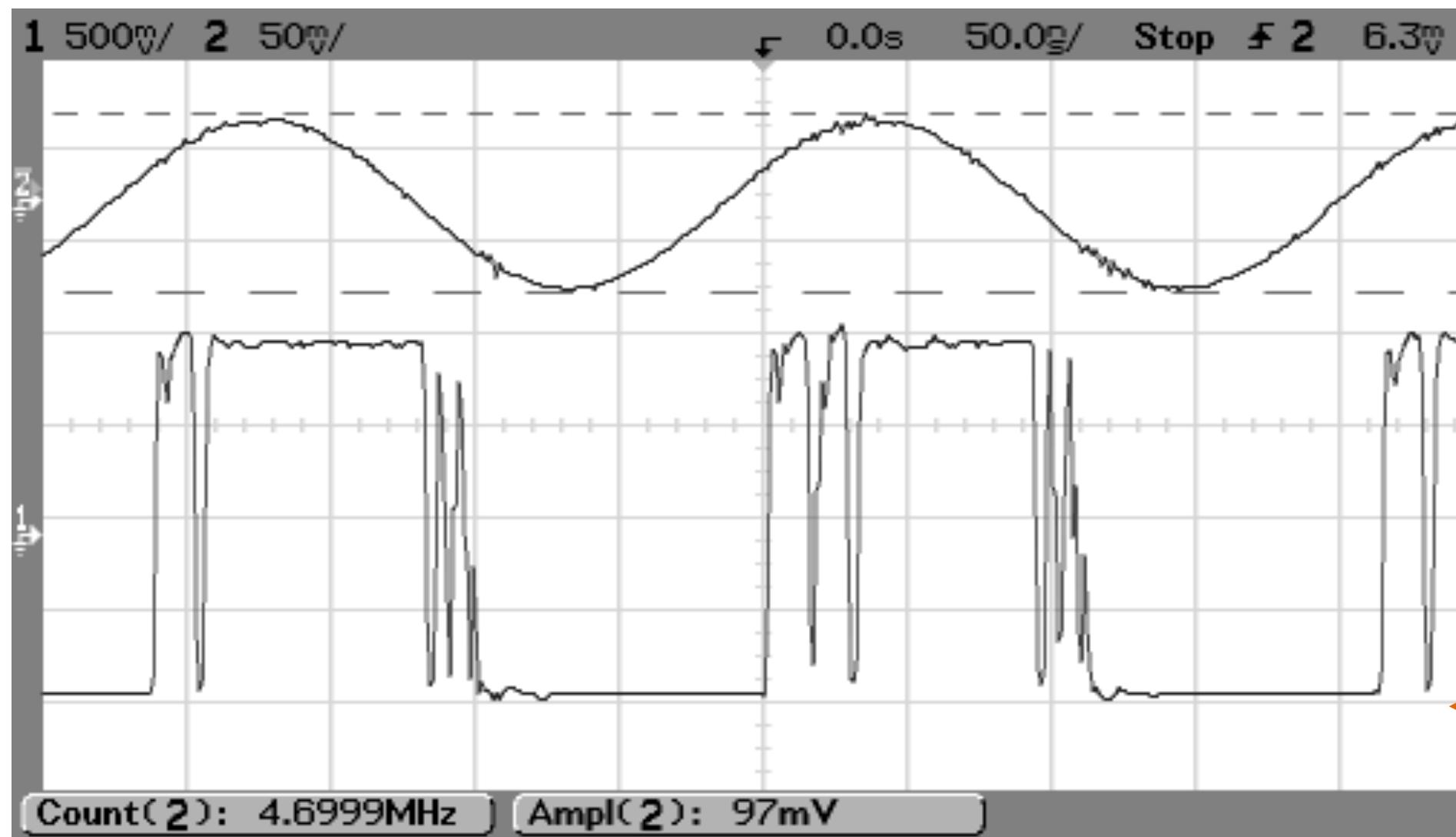
$$\nu_0^2 = \frac{1}{3} \frac{S_v B^3}{V_0^2}$$

Example

- $V_0 = 100 \text{ mV peak}$
- $10 \text{ nV}/\sqrt{\text{Hz}}$ noise
- 650 MHz max \rightarrow 2 GHz noise BW
- Chatter threshold $\nu = 5.2 \text{ MHz}$

Input Chatter – Example

Good agreement with theory

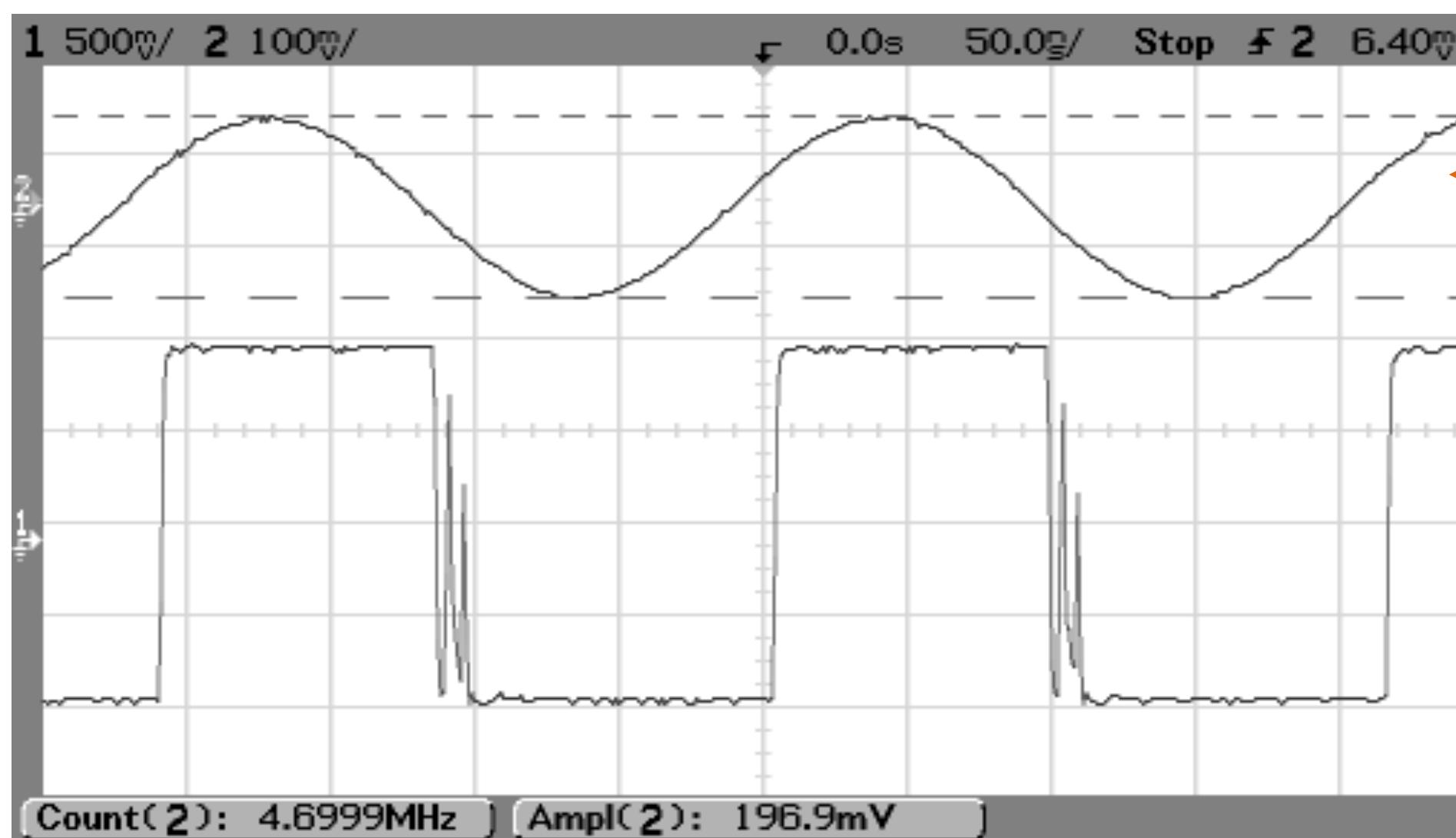


Experiment

- Cyclone III FPGA
- Estimated noise $10 \text{ nV}/\sqrt{\text{Hz}}$
- Estimated BW 2 GHz

$$\leftarrow V_0 = 50 \text{ mV} (100 \text{ mV}_{\text{pp}})$$

$$v_0 = 4.7 \text{ MHz}$$



$$\leftarrow V_0 = 100 \text{ mV} (200 \text{ mV}_{\text{pp}})$$

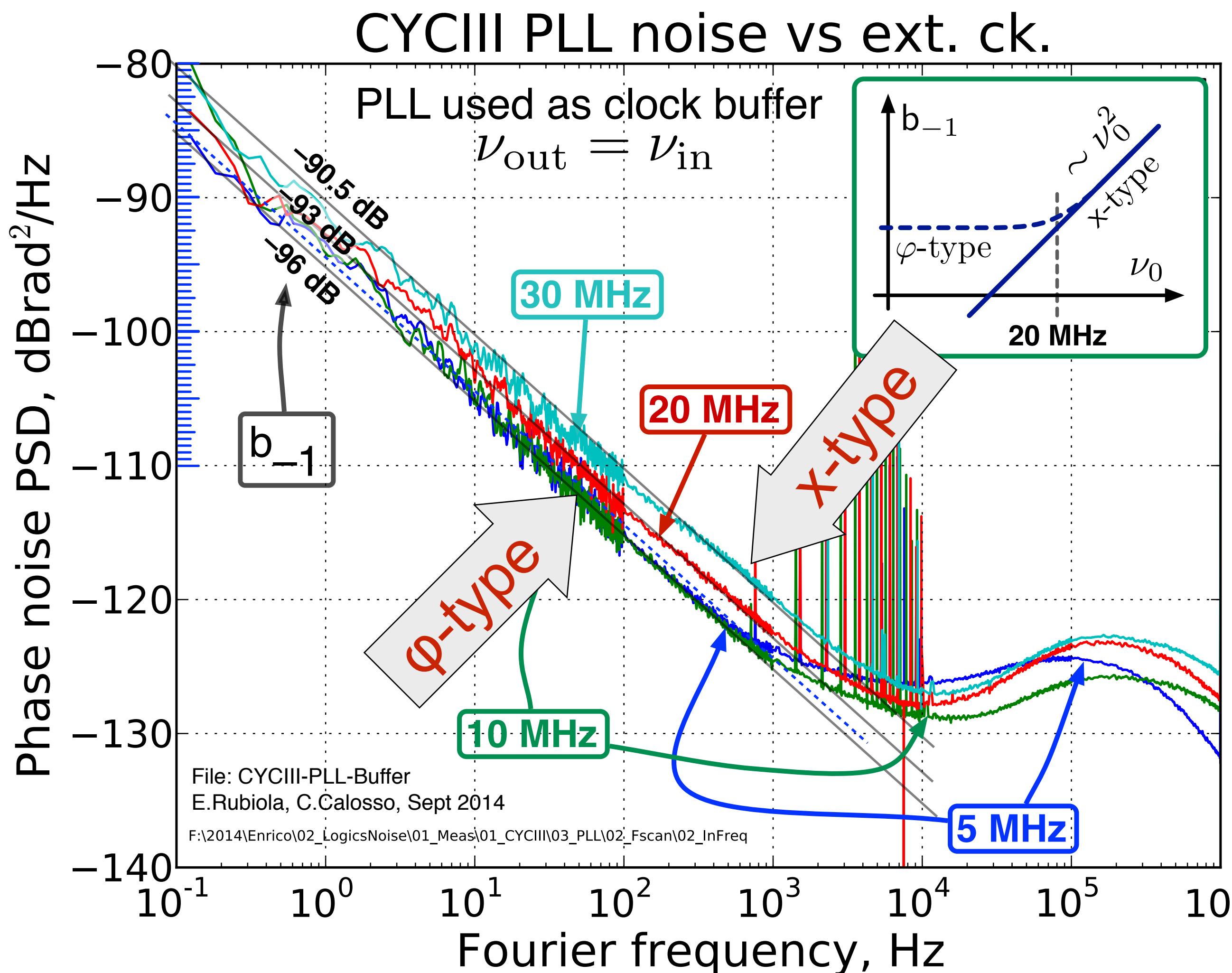
$$v_0 = 4.7 \text{ MHz}$$

Asymmetry shows up

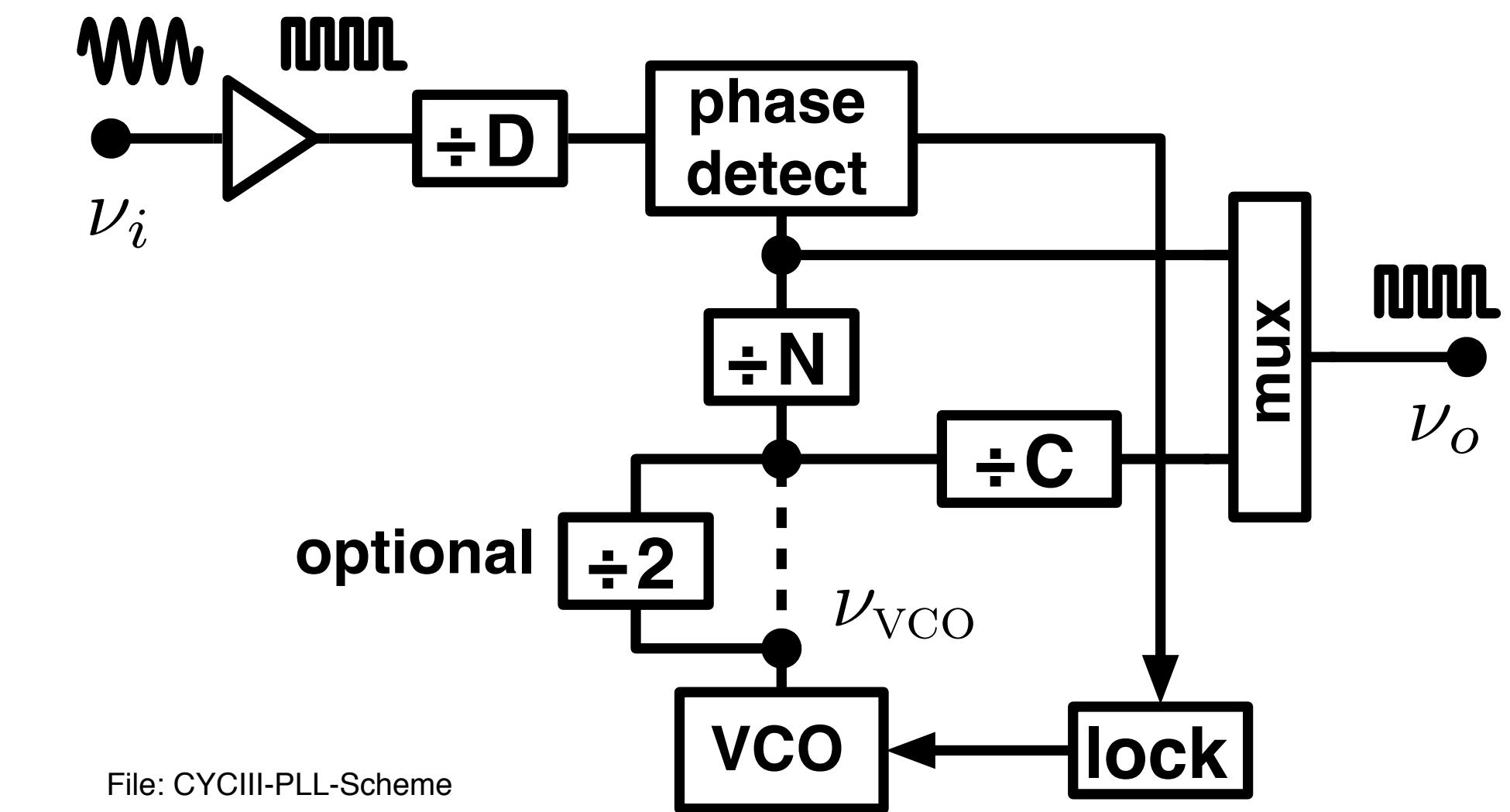
Explanation takes a detailed electrical model, which we have not

Cyclone III Internal PLL

PLL used as a buffer



x-type → analog noise in the phase detector

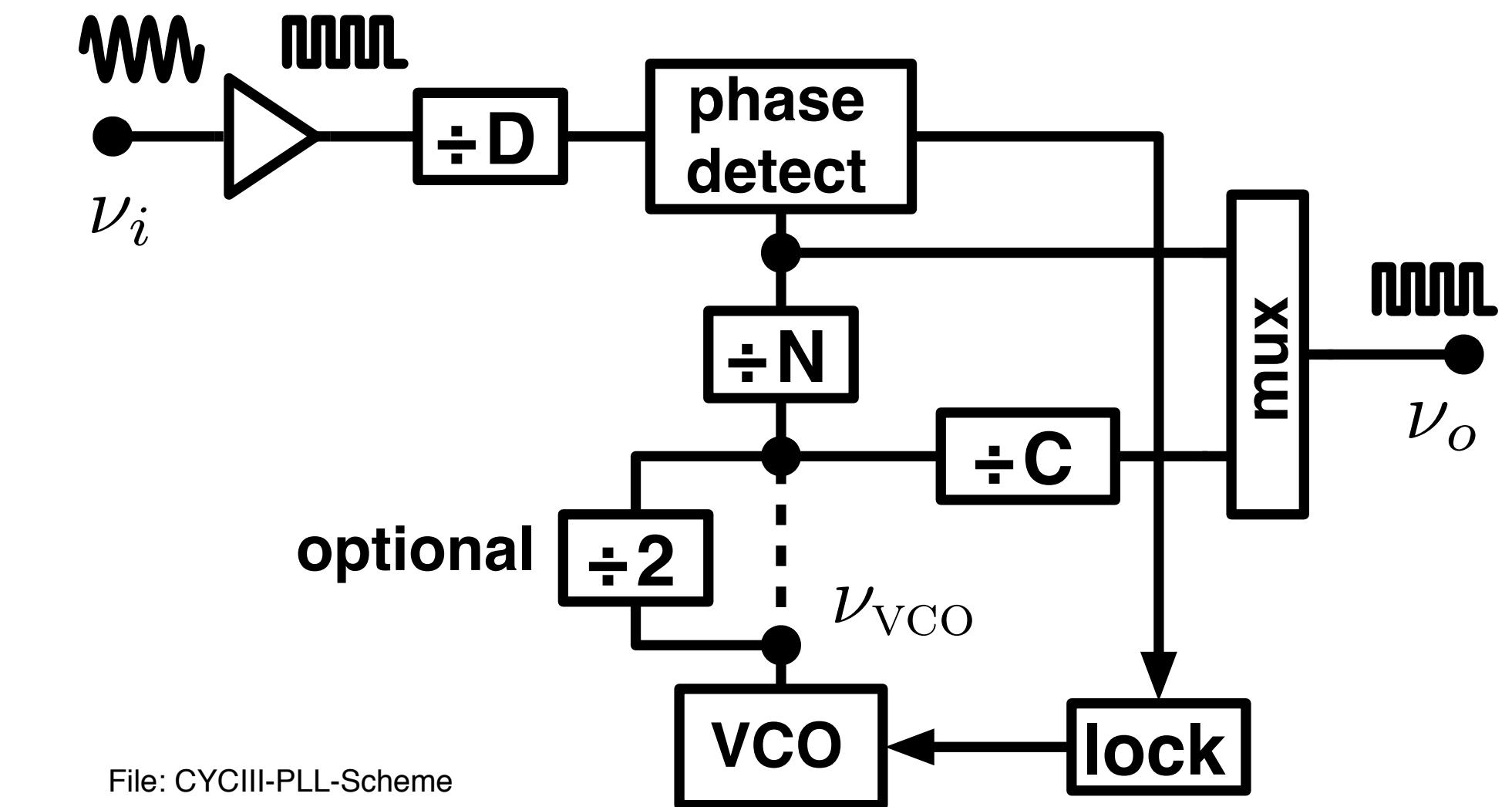
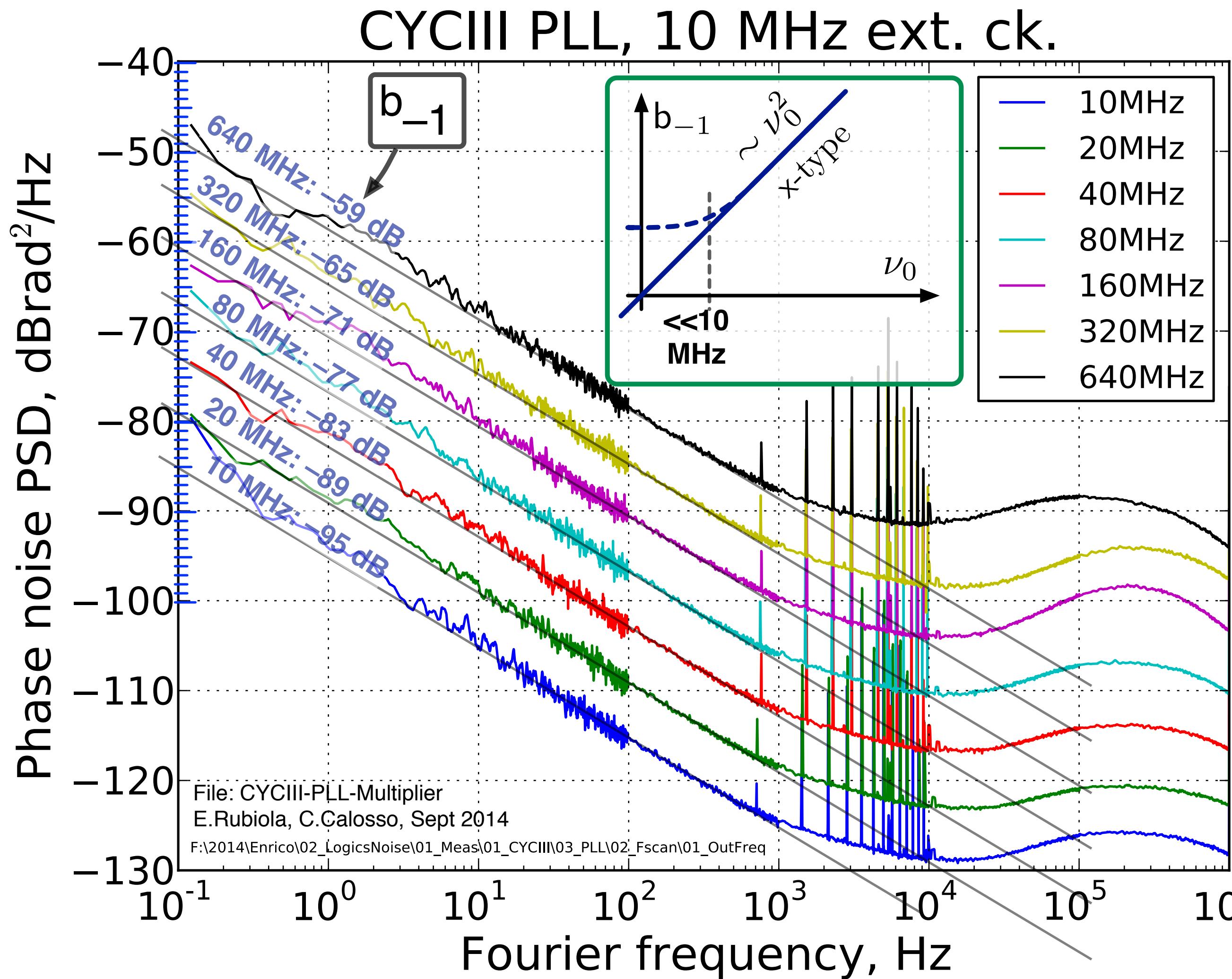


- LC oscillator, 0.6–1.3 GHz, $Q \approx 10$
- Optional $\div 2$ always present
- We set $D = 1$ (for lowest noise)
- QUARTUS app chooses C and N

Crossover between phi-type and x-type at 20 MHz

Cyclone III Internal PLL

PLL used as a frequency multiplier

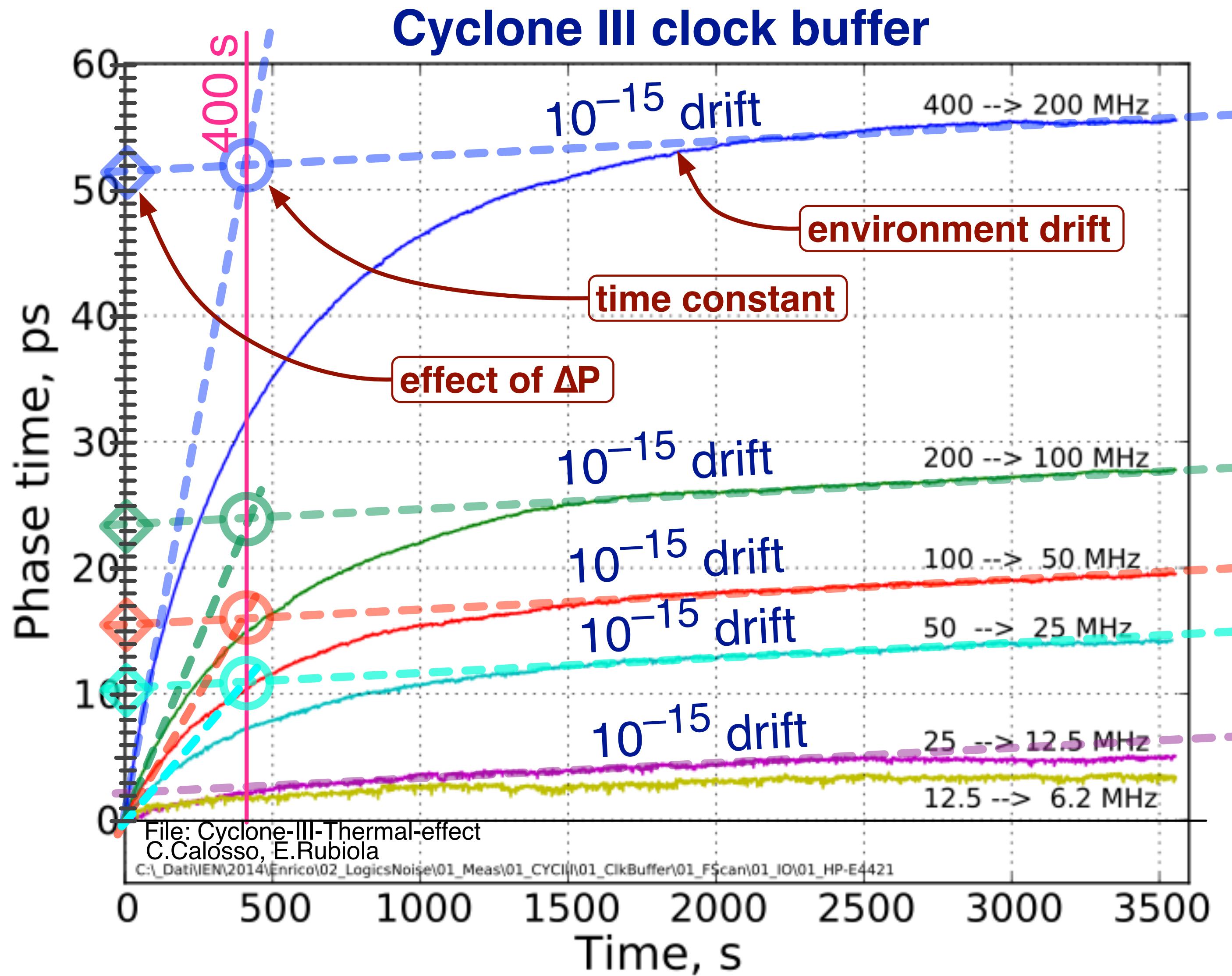


10 MHz input, $N \times 10$ MHz out

- $1/f$ phase noise is dominant
- Scales as $N^2 \rightarrow$ analog noise in the phase detector
- ADEV 1.5×10^{-12} @ 1 s, $f_H = 500$ Hz

$$-115 \text{ dB} + 20 \log_{10}(v_0), \quad v_0 \text{ in MHz}$$

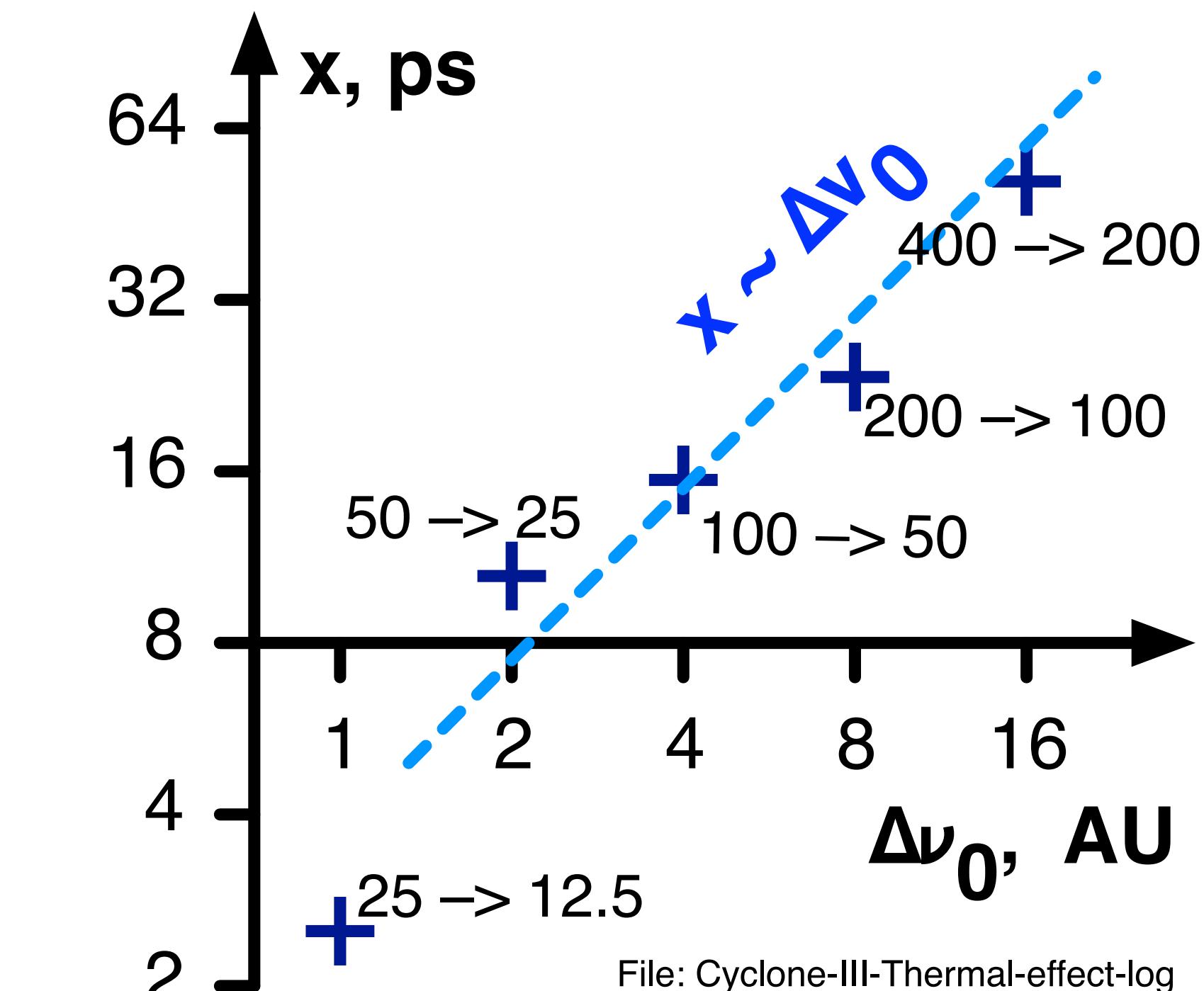
Thermal Effects



Gate power

$$P = CV_{CC}^2 \nu_c$$

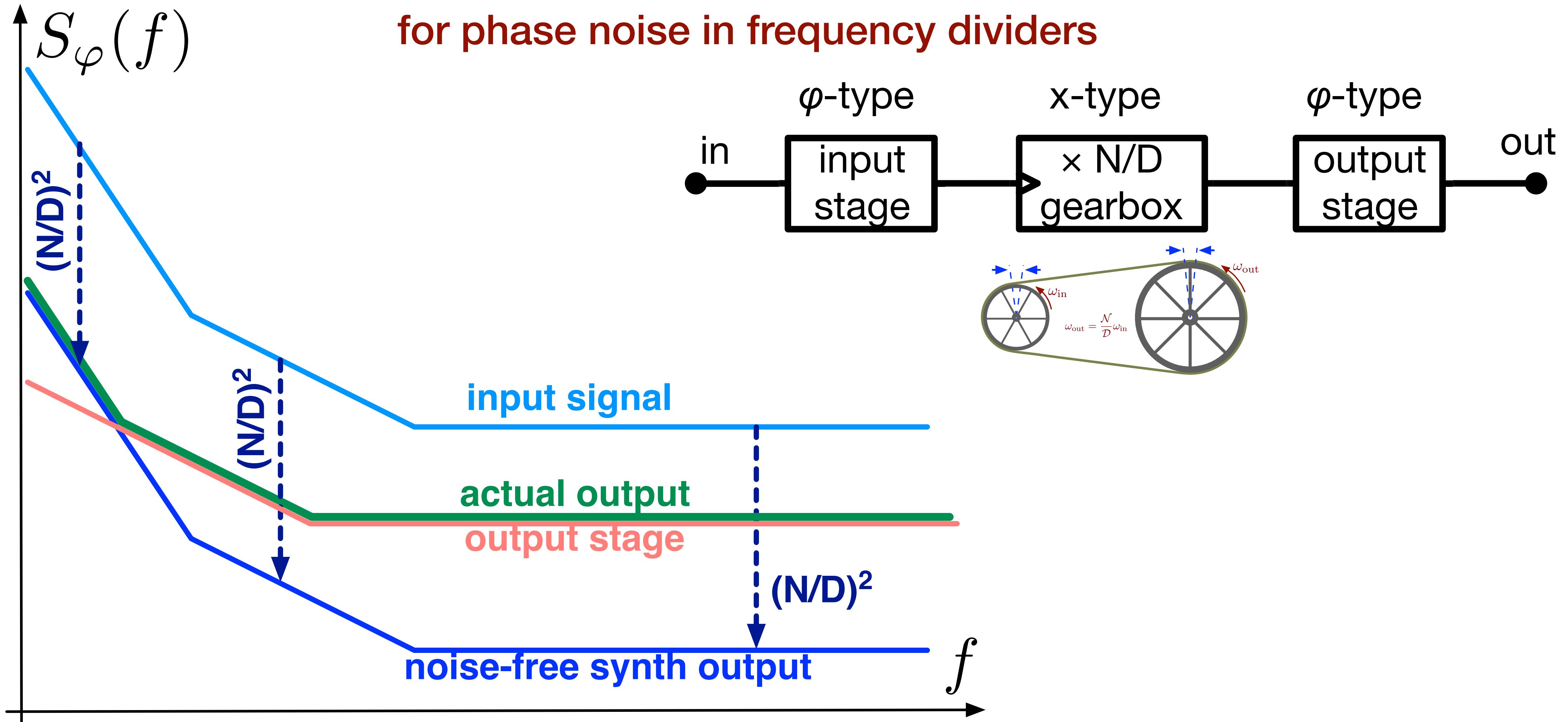
C



In real applications, other parts of the same FPGA impact on the temperature

Frequency Synthesis

The Egan Model – Modern View



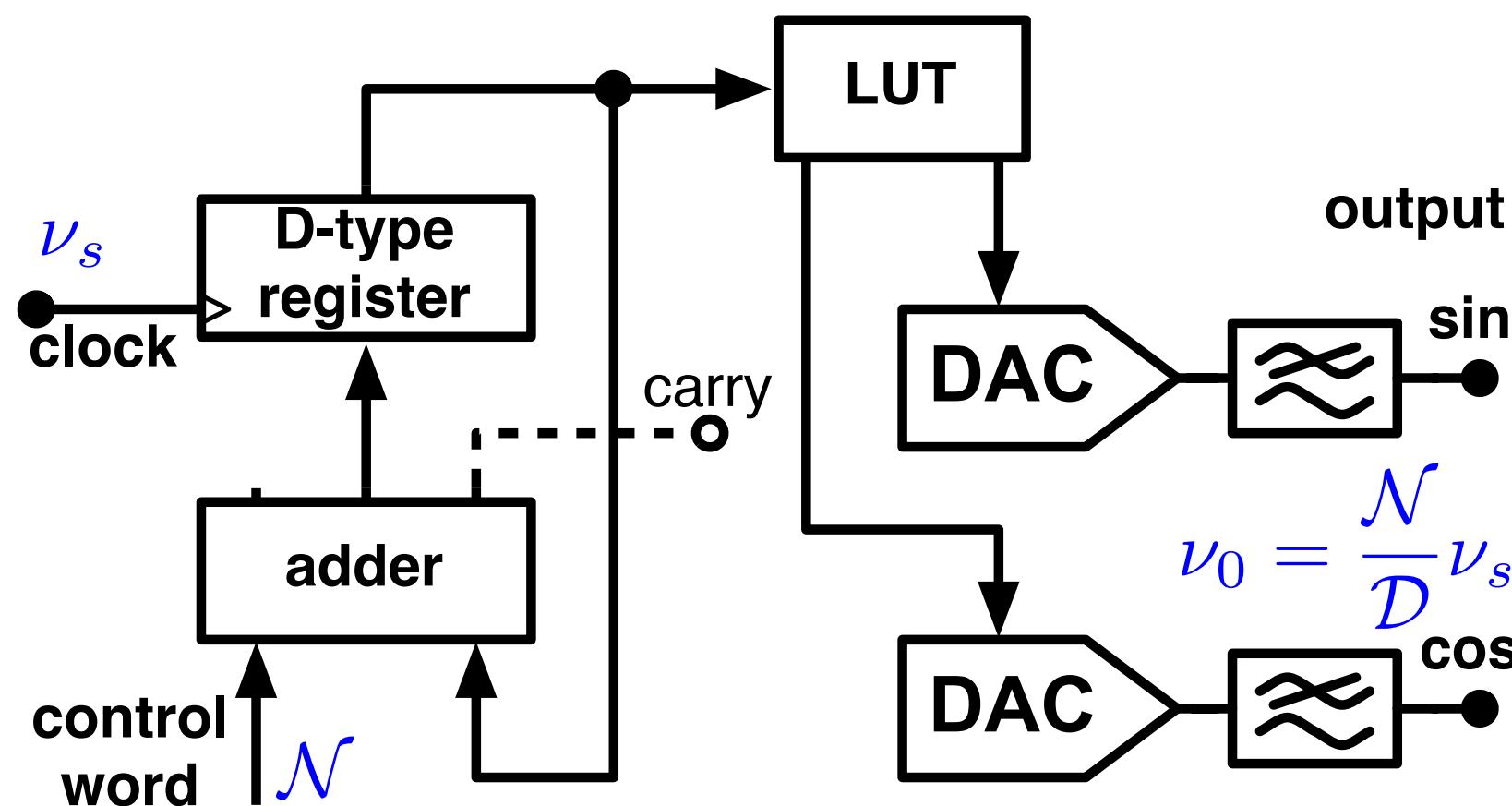
For $N/D \ll 1$, the scaled-down noise hits the output-stage limit

DDS

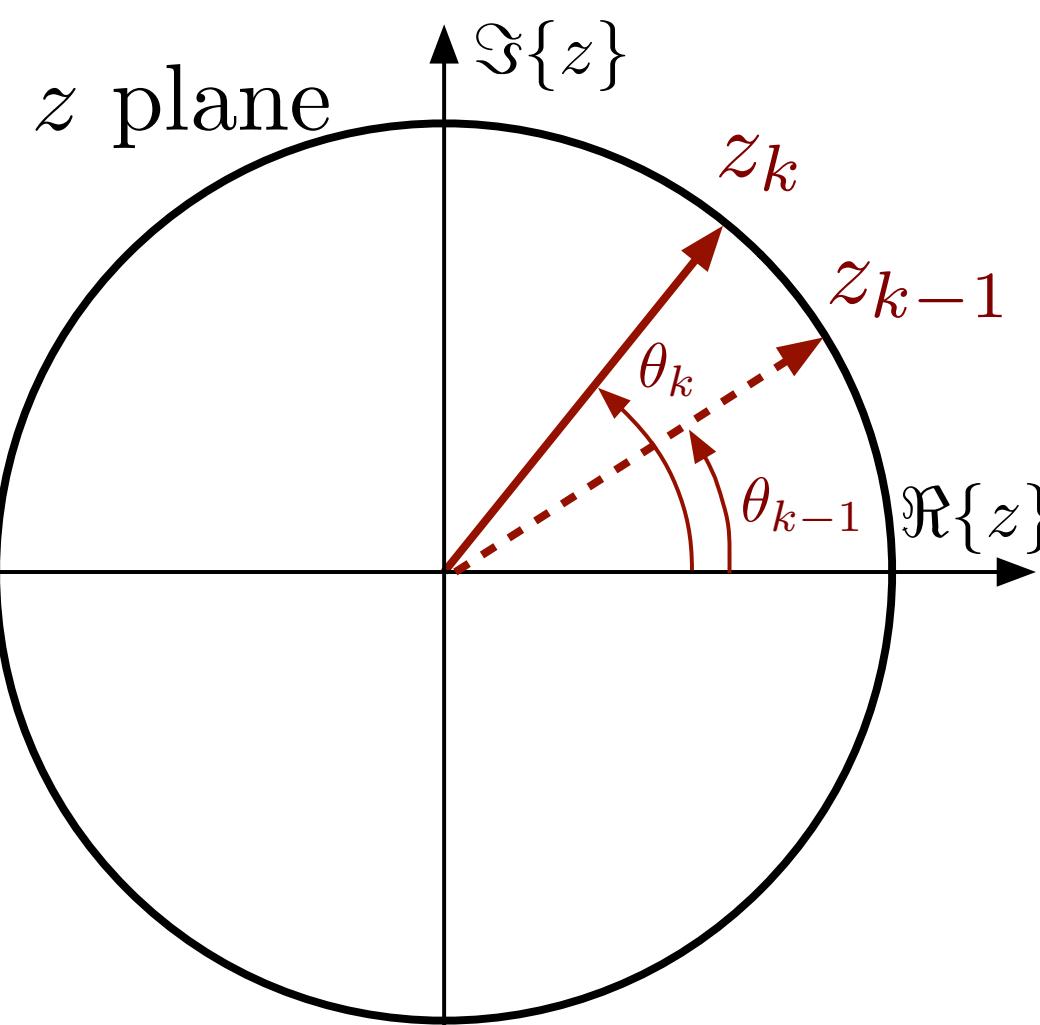
Basic DDS Scheme

replace
 $\theta \rightarrow \phi$

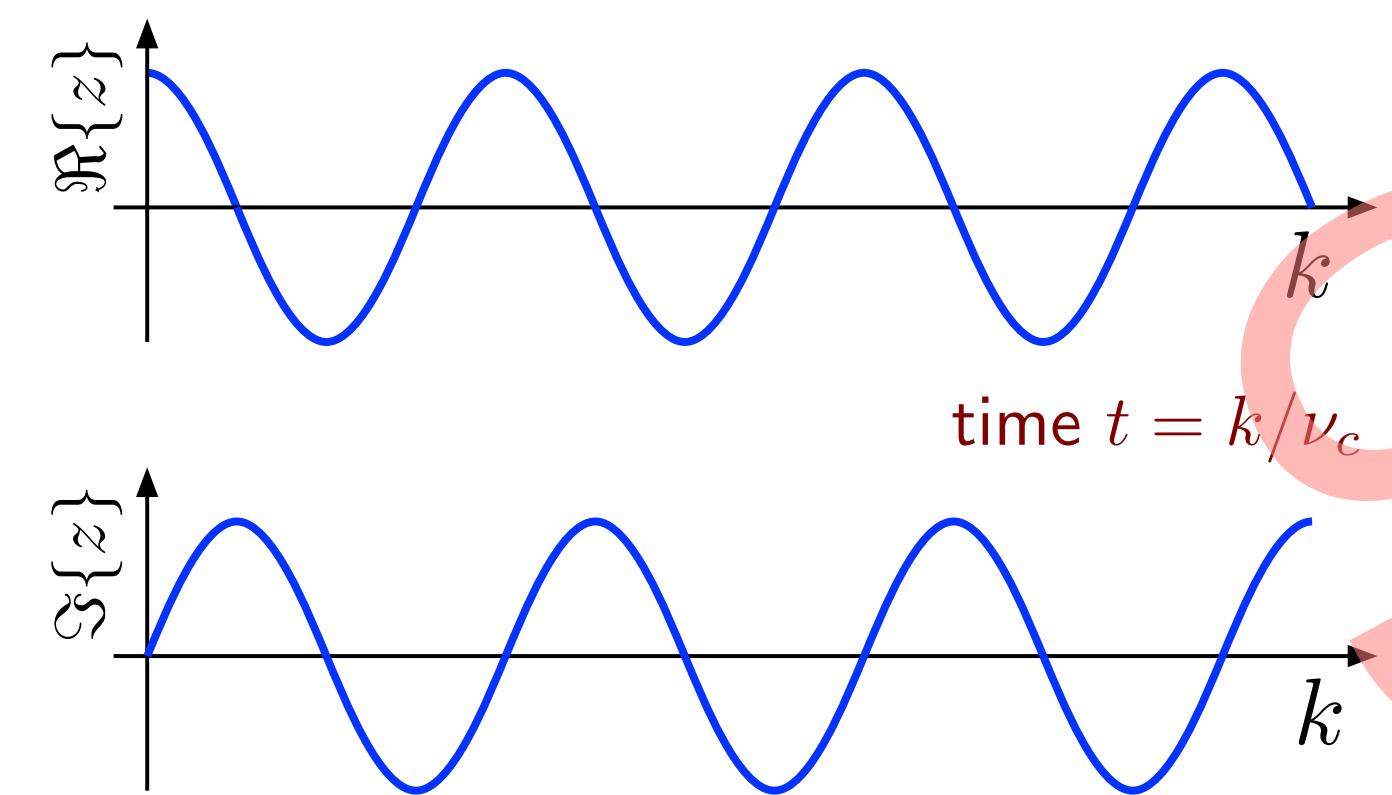
integer: $n_k = (n_{k-1} + \mathcal{N}) \bmod \mathcal{D}$
 complex: $z_k = z_{k-1} \exp(j\eta)$
 phase: $\theta_k = (\theta_{k-1} + \eta) \bmod 2\pi$



quantity	digital	analog
state variable	n	$\theta = 2\pi \frac{n}{\mathcal{D}}$
assoc. complex		$z = e^{j\theta}$
modulo	$\mathcal{D} = 2^m$	2π
increment	\mathcal{N}	$\eta = 2\pi \frac{\mathcal{N}}{\mathcal{D}}$
time	$k, 0, 1, 2, \dots$	$t = k/\nu_s$
clock freq. ν_s		output freq. $\nu_0 = \frac{\mathcal{N}}{\mathcal{D}} \nu_s$



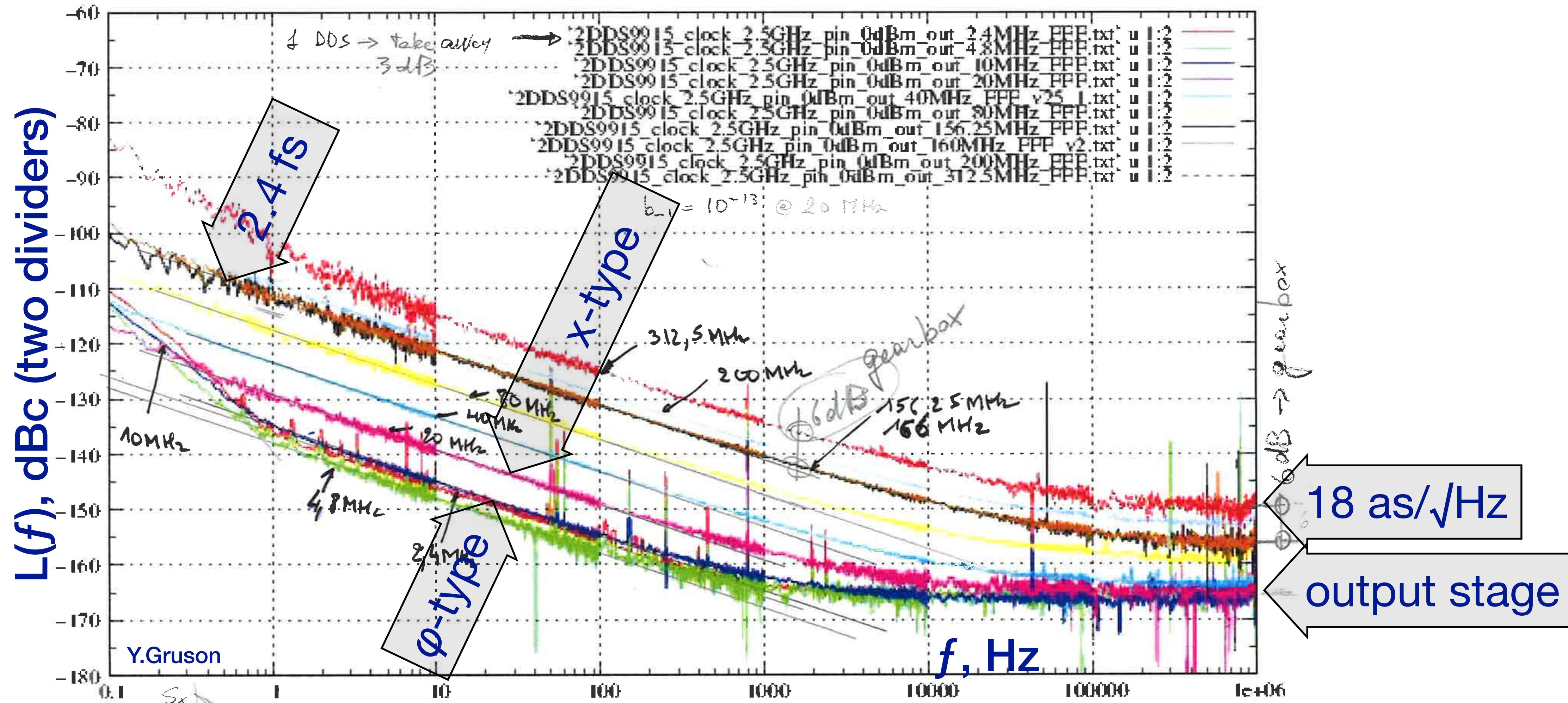
The contents n of the m -bit register is interpreted as a complex number



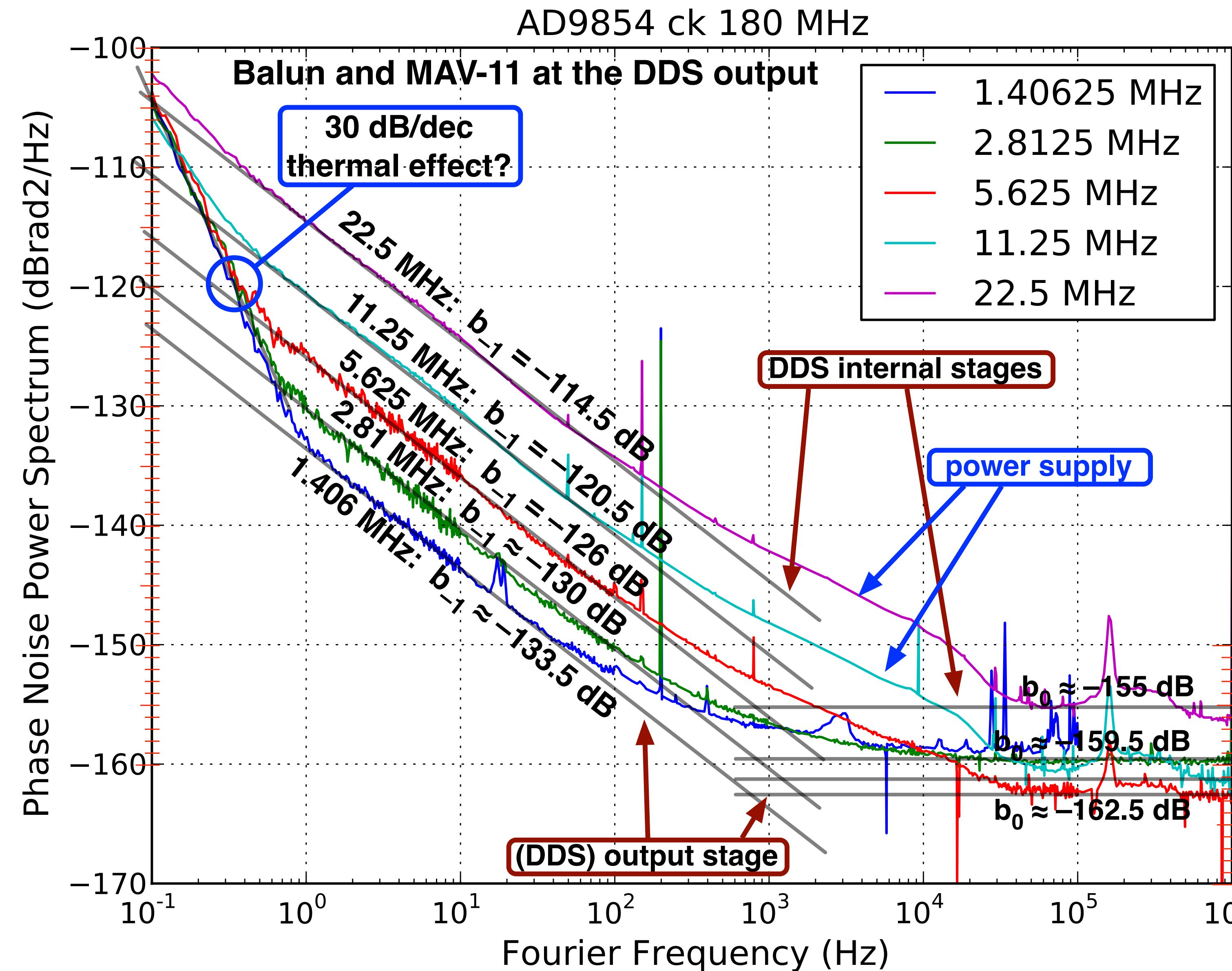
SKIP

High-Frequency DDSs

AD9915 12 bit, 2.5 GHz
64 bit accumulator (135 pHz res)



PM Noise vs Output Frequency



AD 9912 PM Noise

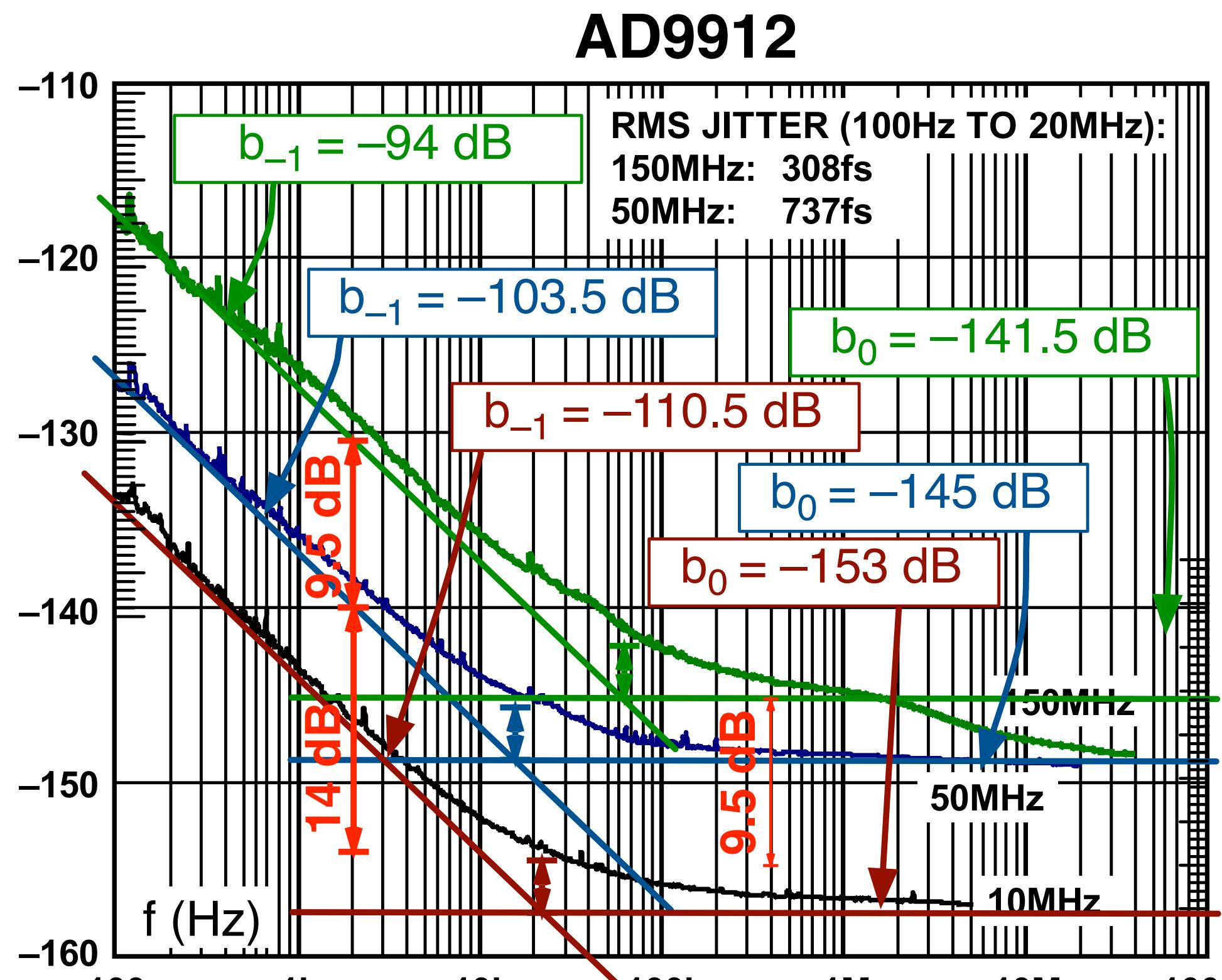
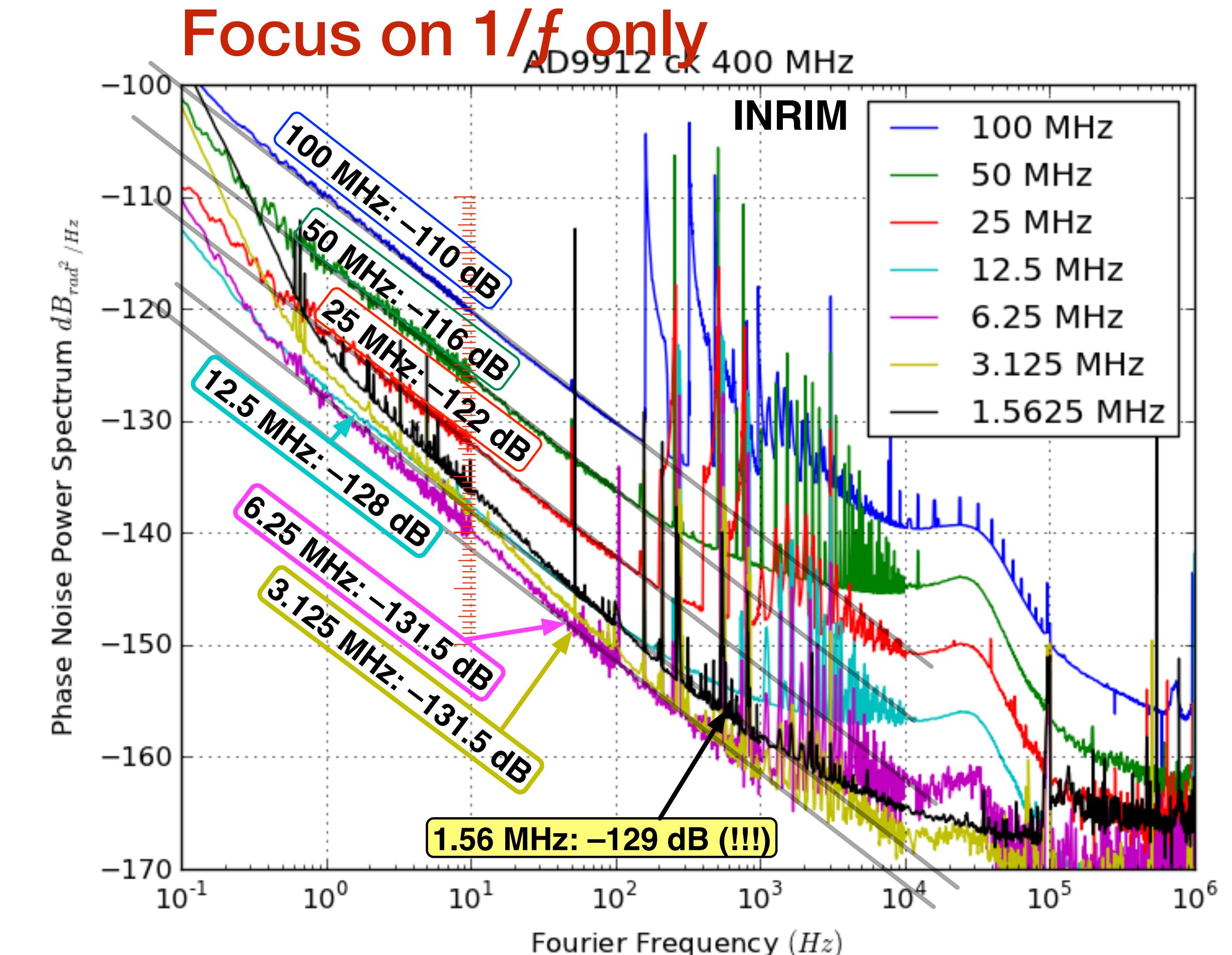


Figure 16. Absolute Phase Noise Using CMOS Driver at 3.3 V,
SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)
DDS Run at 200 MSPS for 10 MHz



- At 50 MHz and 10/12.5 MHz we get ≈ 15 dB lower flicker than the data-sheet spectrum
- Experimental conditions unclear in the data sheets

3.3 V: Lower PM Noise than 1.8 V

Probably related to the cell size and to the dynamic range

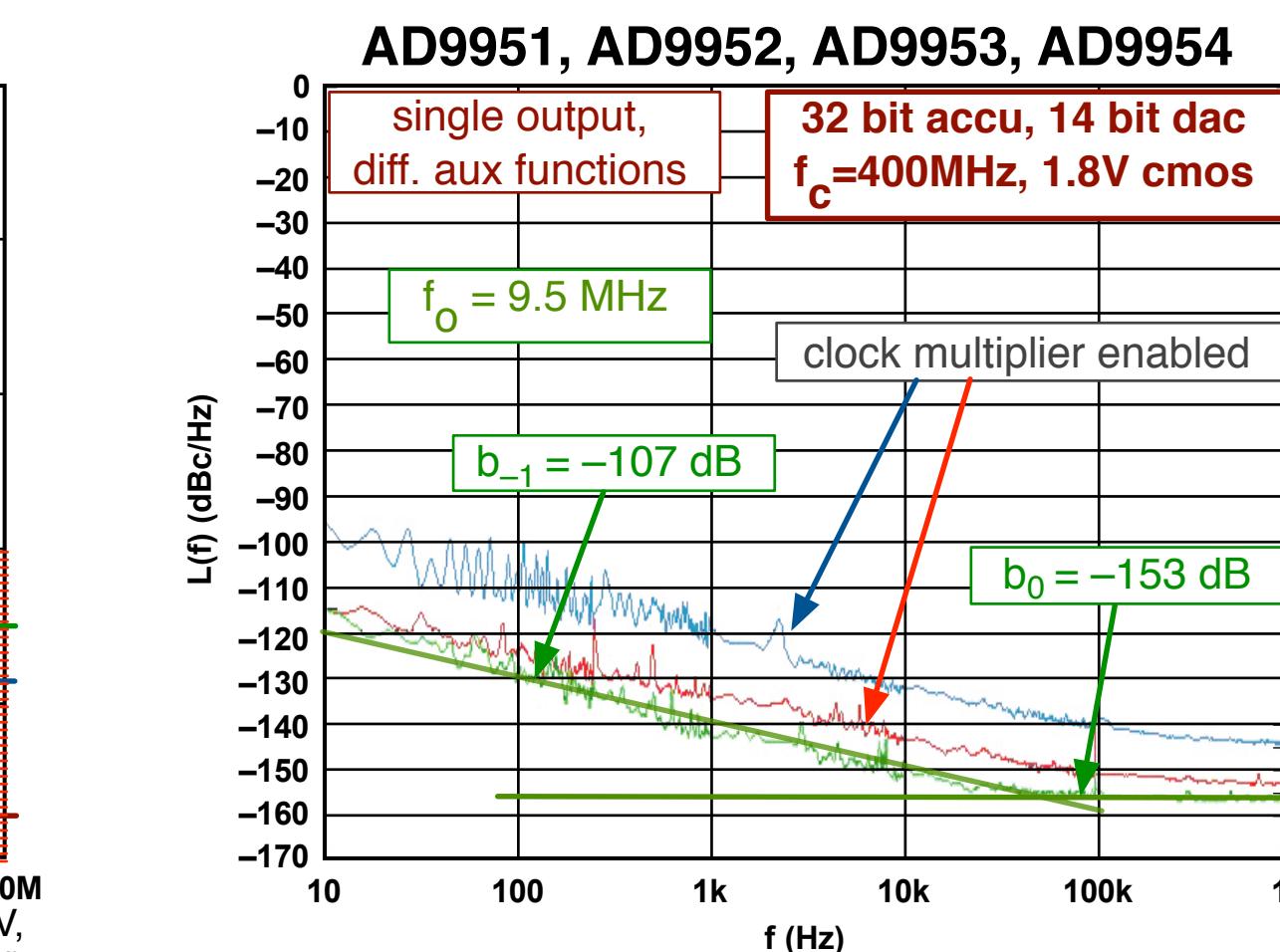
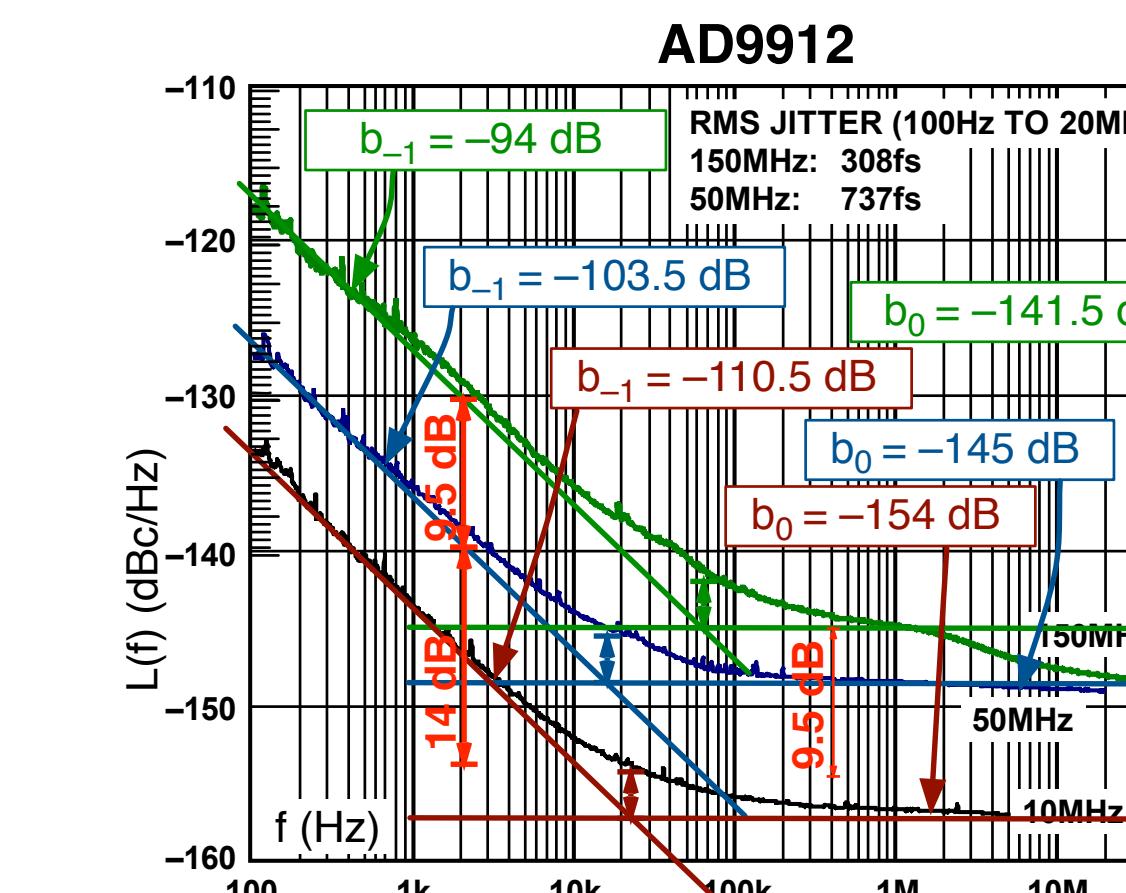
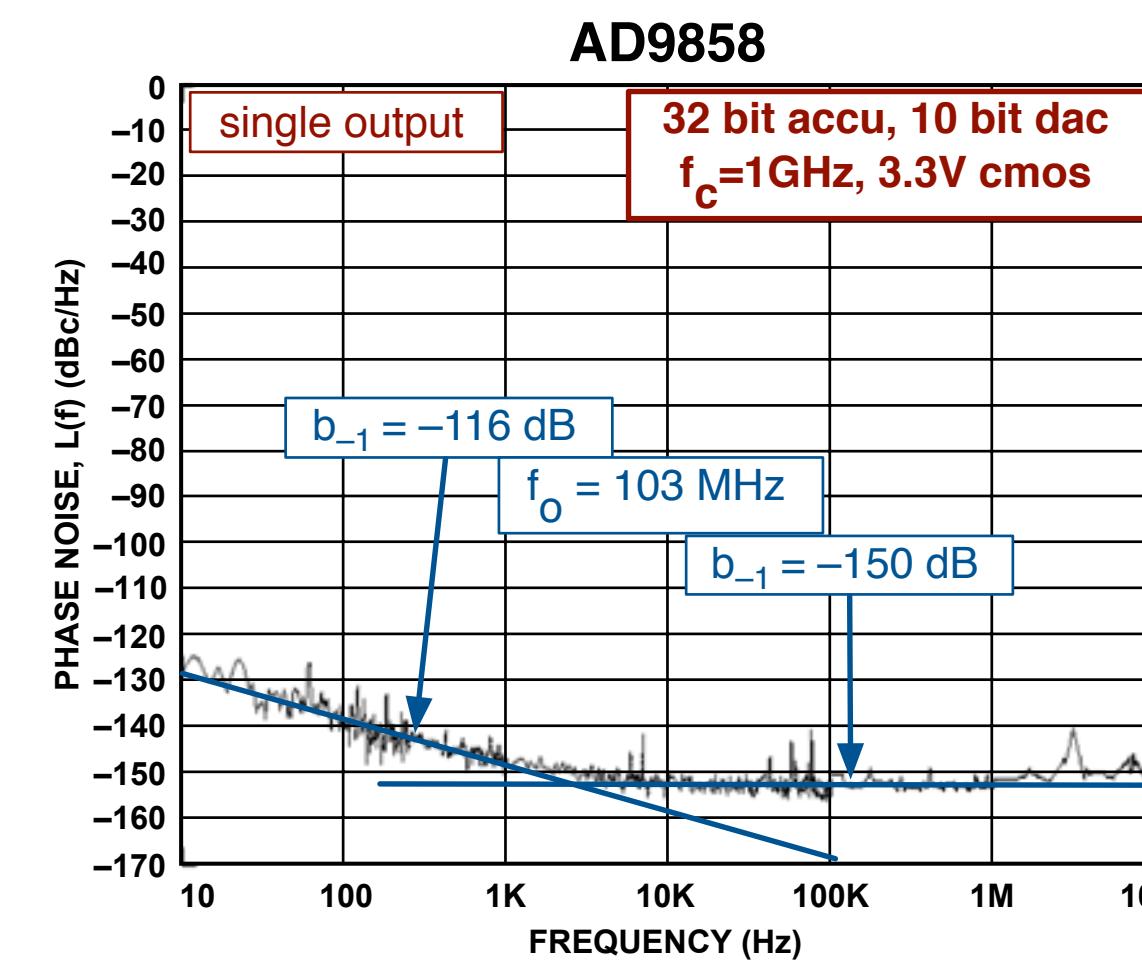
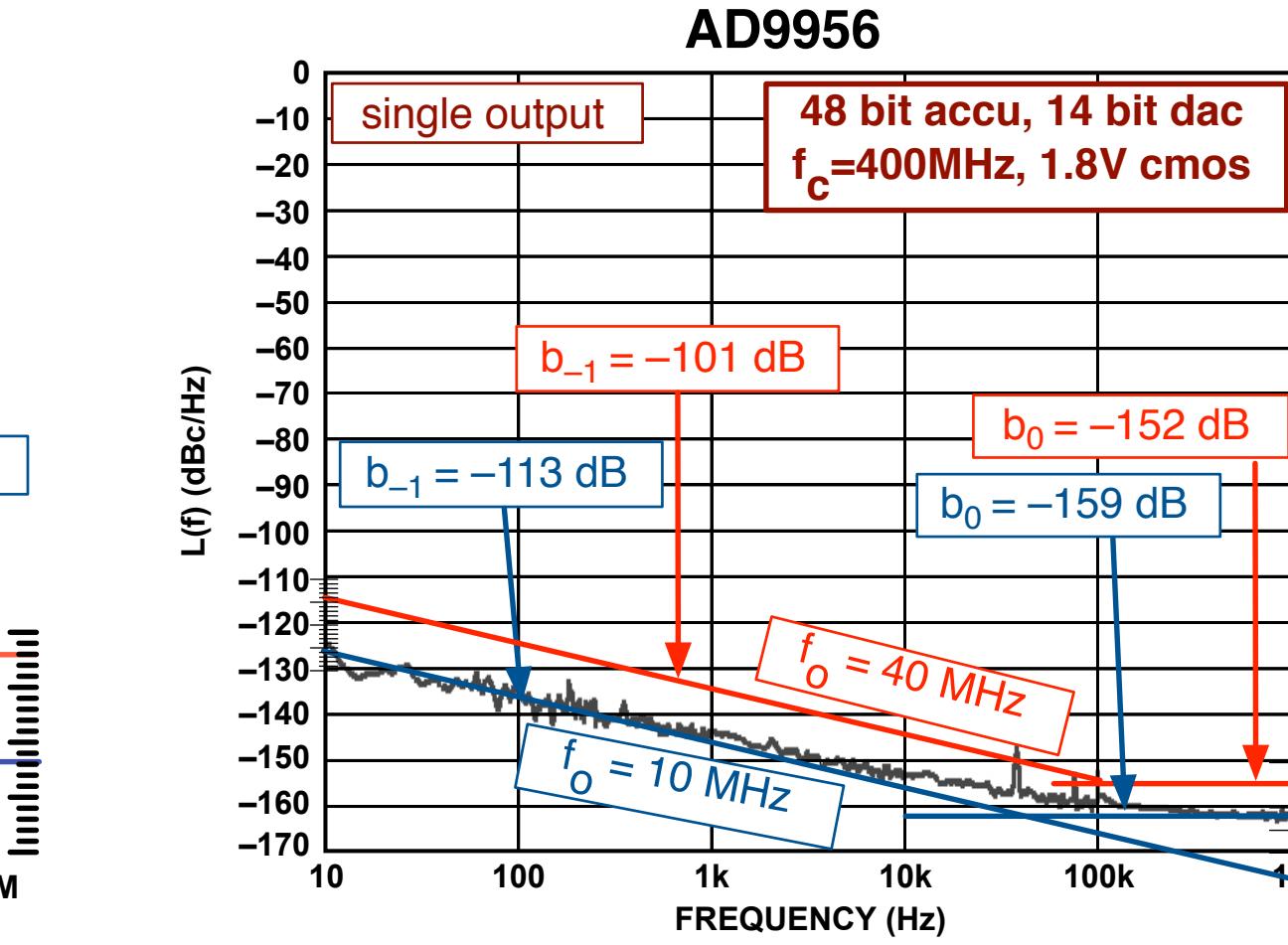
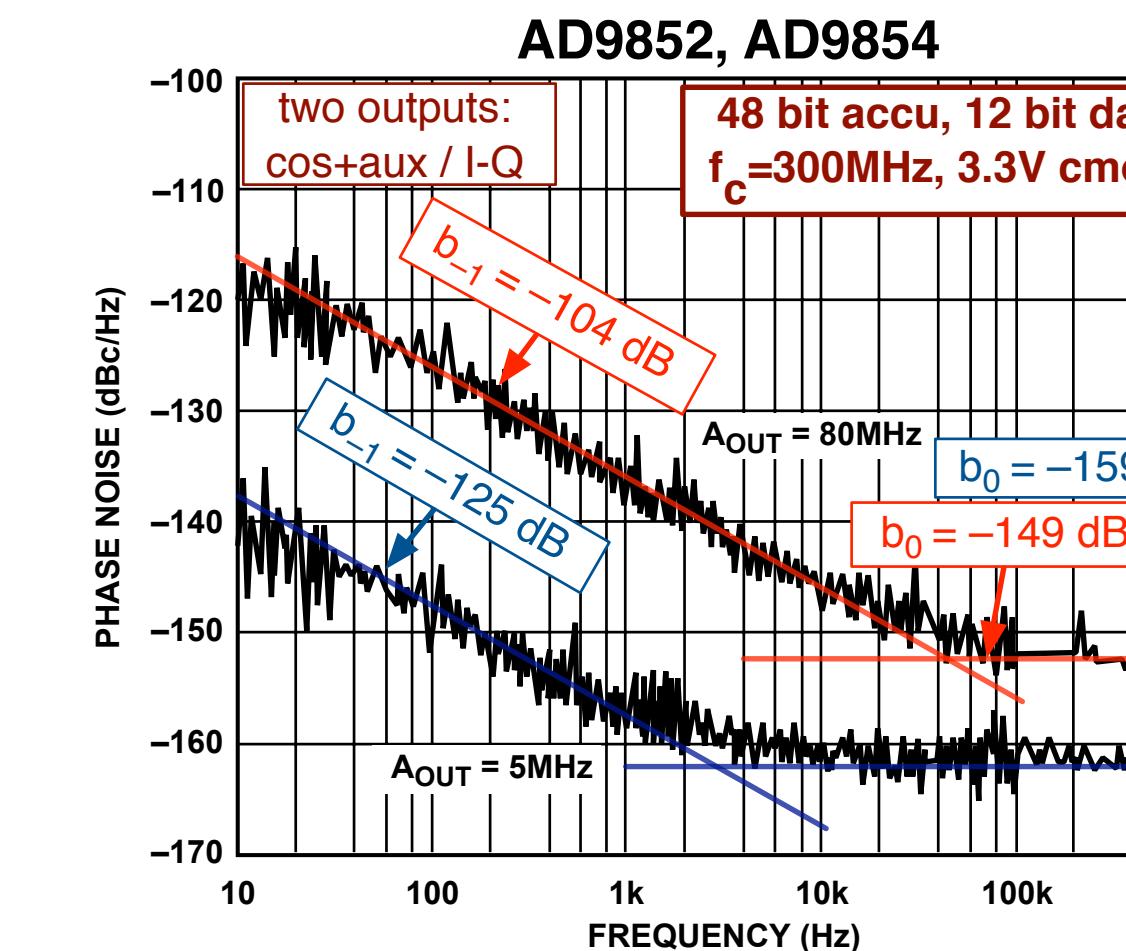
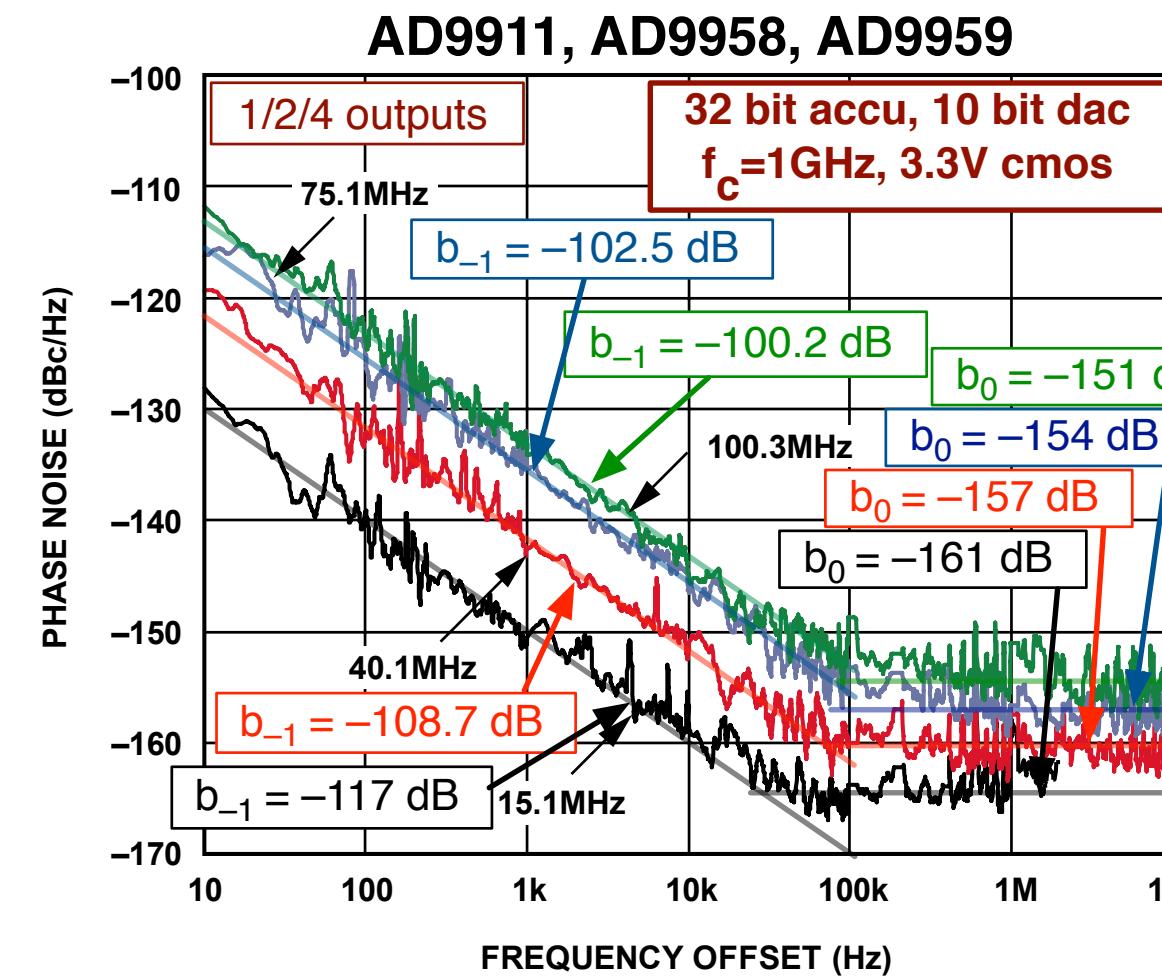
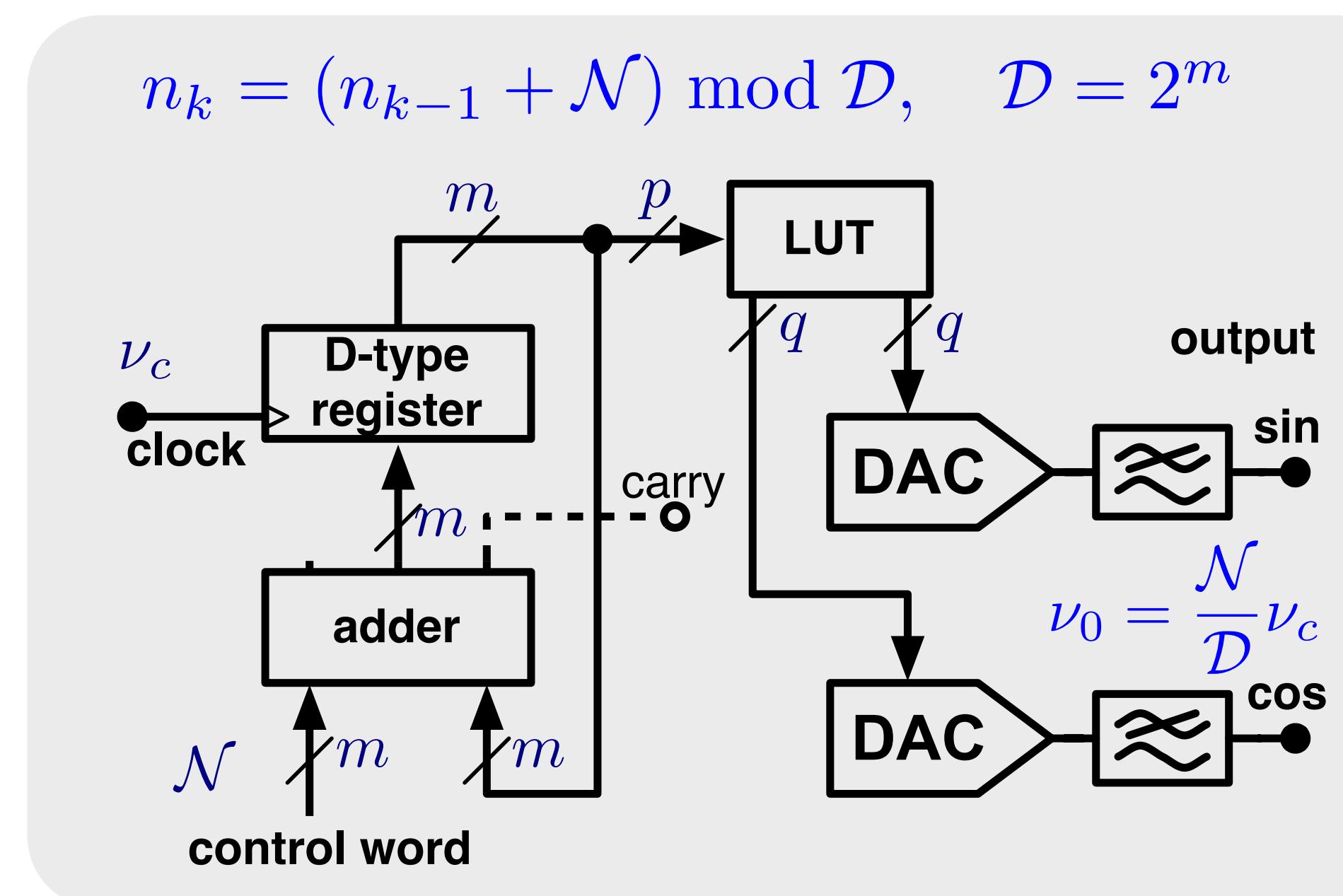


Figure 16. Absolute Phase Noise Using CMOS Driver at 3.3 V,
SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)
DDS Run at 200 MSPS for 10 MHz

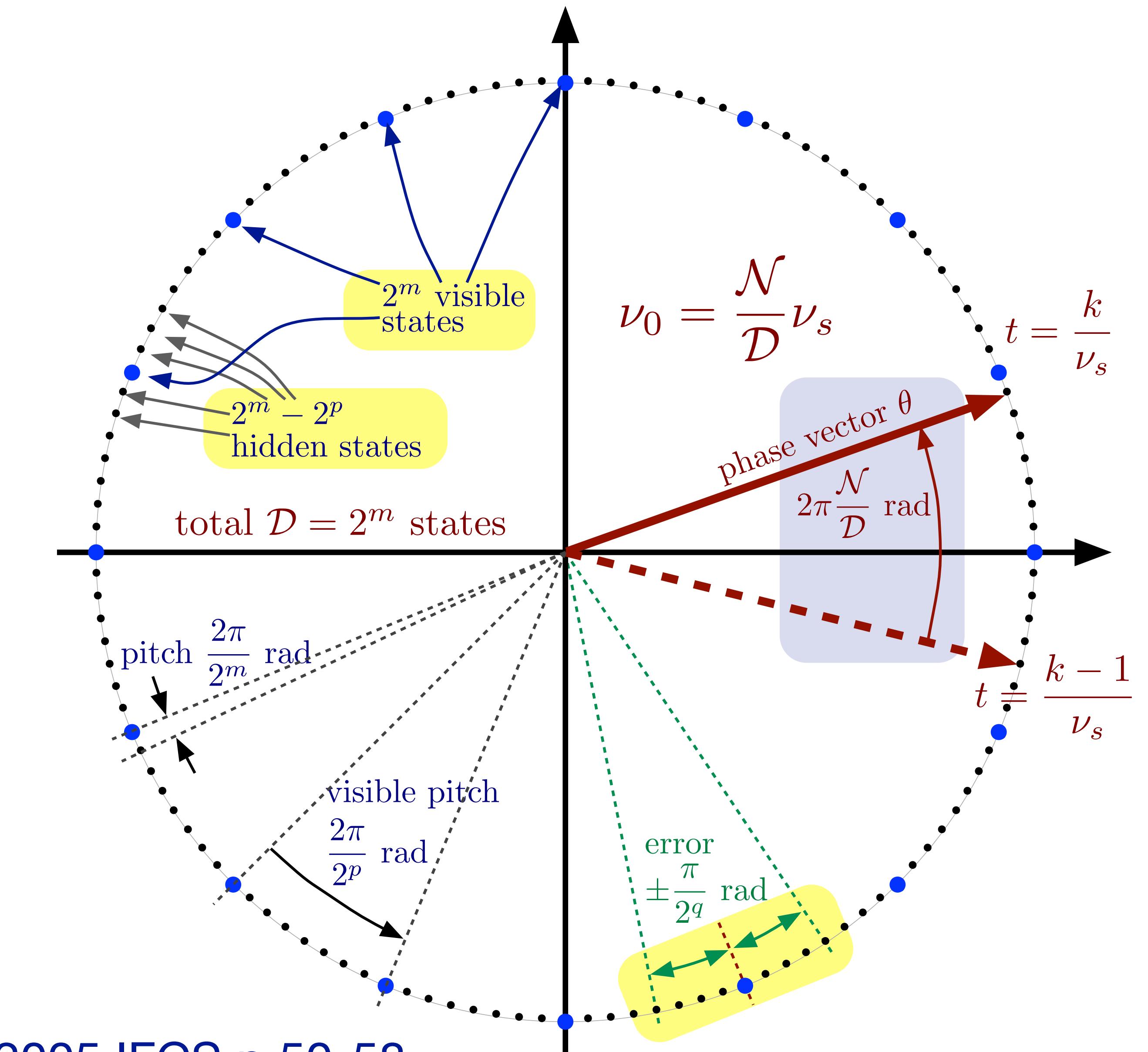
E. Rubiola, Mar 2007 (adapted from the Analog Devices data sheets)

Plots originally used to extract the noise parameters

State-Variable Truncation

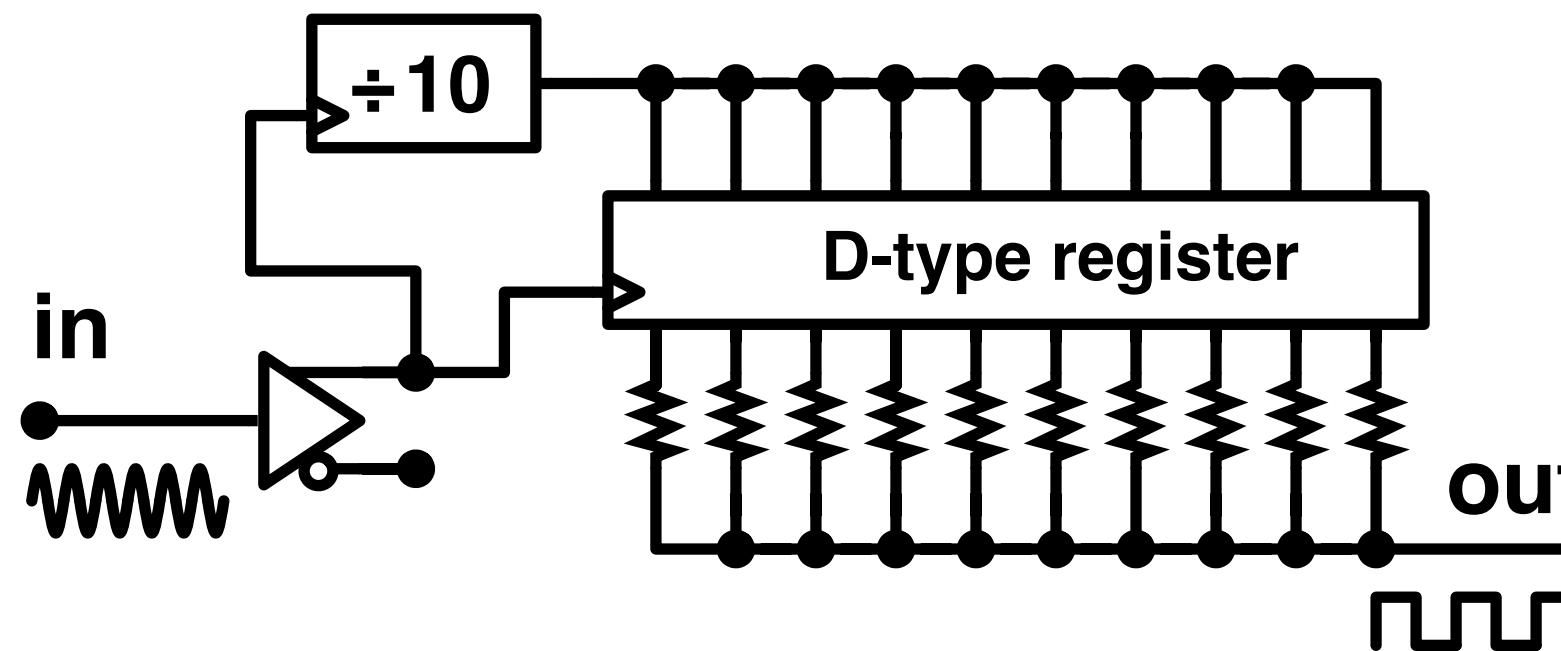


- Only quantization shows up with full m-bit conversion
- Technology \rightarrow q max
- Why $p > q$
- Slow pseudorandom beat,
3d 6h 11m 15s @ 1 GHz, 48 bit

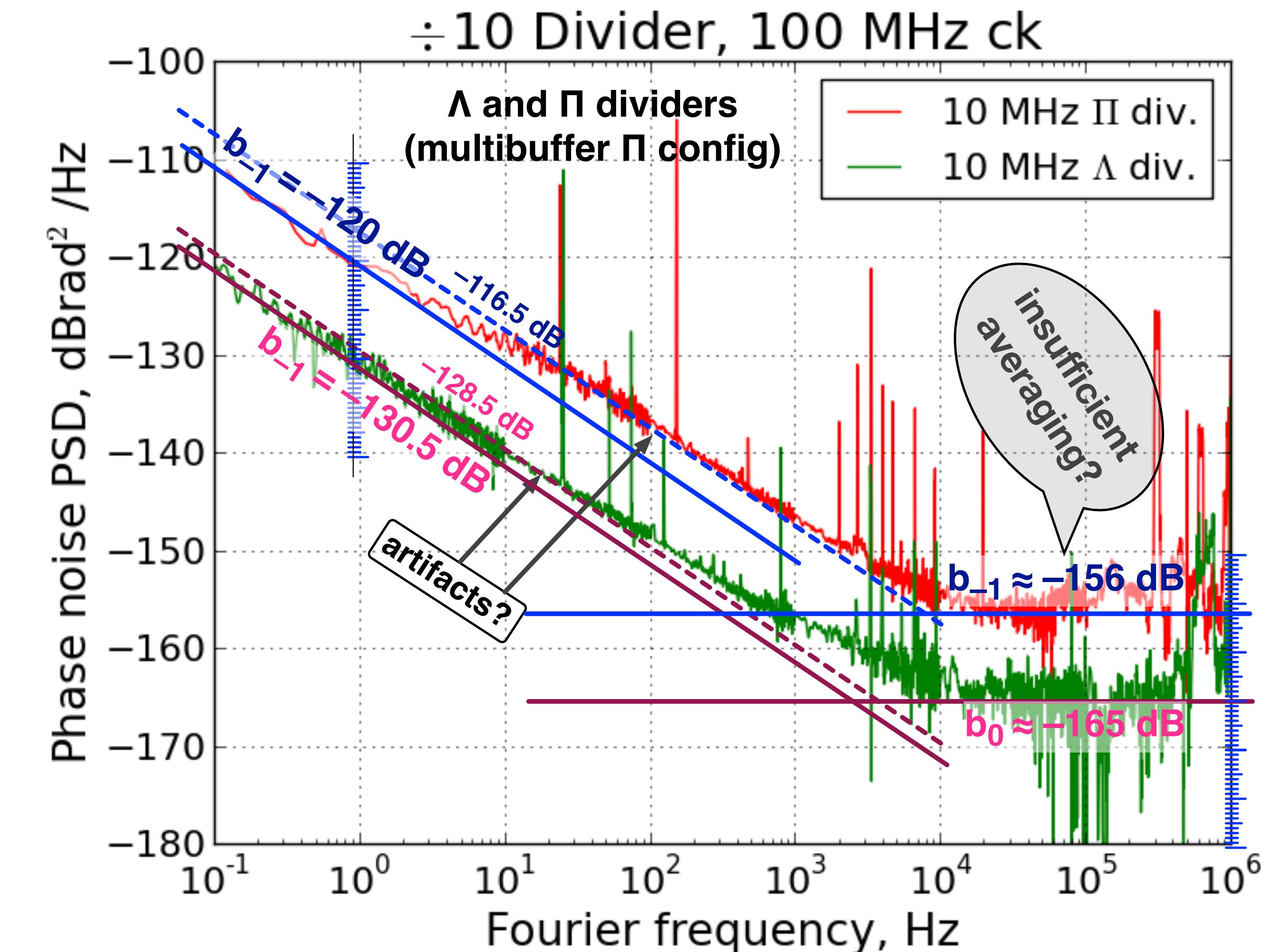
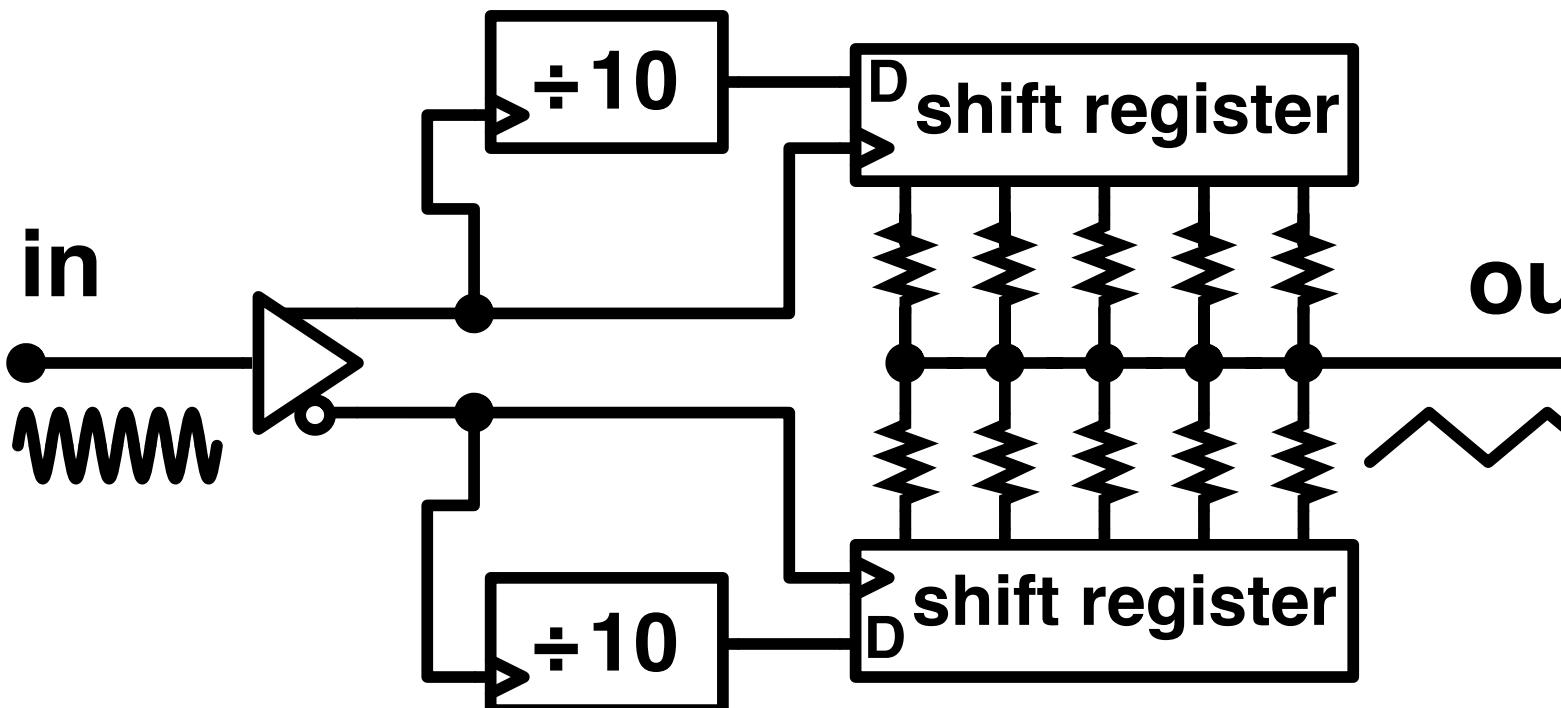


Phase Noise of Π and Λ Dividers

Multibuffer Π divider
Aliasing is present



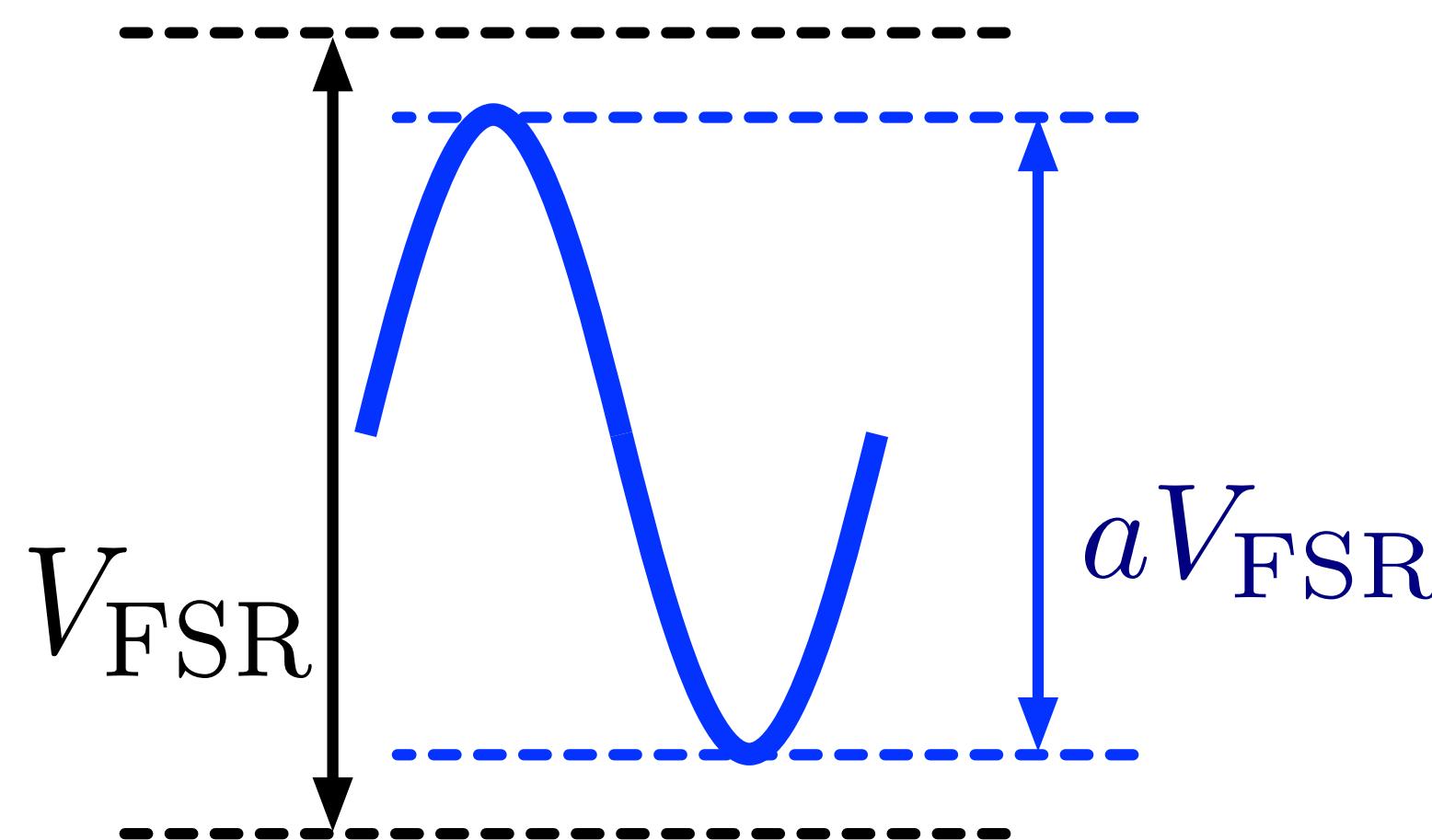
Λ divider
High-f sampling removes aliasing



experimental problems still present

ADCs

Quantization & Sinusoidal Signals



Assume that the noise power is equally distributed between 0 and $B = f_s/2$

This is not true when signal and clock are highly coherent (Widrow-Kollar, Appendix G)

Widrow B, Kollar I - Quantization Noise - Cambridge 2008

$$6.02 M + 1.25 - 10 \log_{10}(f_s) - 10 \log_{10}(a) \text{ dB}$$

Sampling jitter breaks AM/PM symmetry

Signal power

$$P_0 = \frac{V_{pp}^2}{8} = \frac{a^2 V_{FSR}^2}{8}$$

Noise power

$$\sigma^2 = \frac{V_{LSB}^2}{12} \quad \text{SNR} = \frac{3}{2} 2^{2M}, \quad a = 1$$

Parseval theorem, $B = f_s/2$

$$S_v = \frac{\sigma^2}{B} \Rightarrow S_v = \frac{V_{LSB}^2}{6f_s}$$

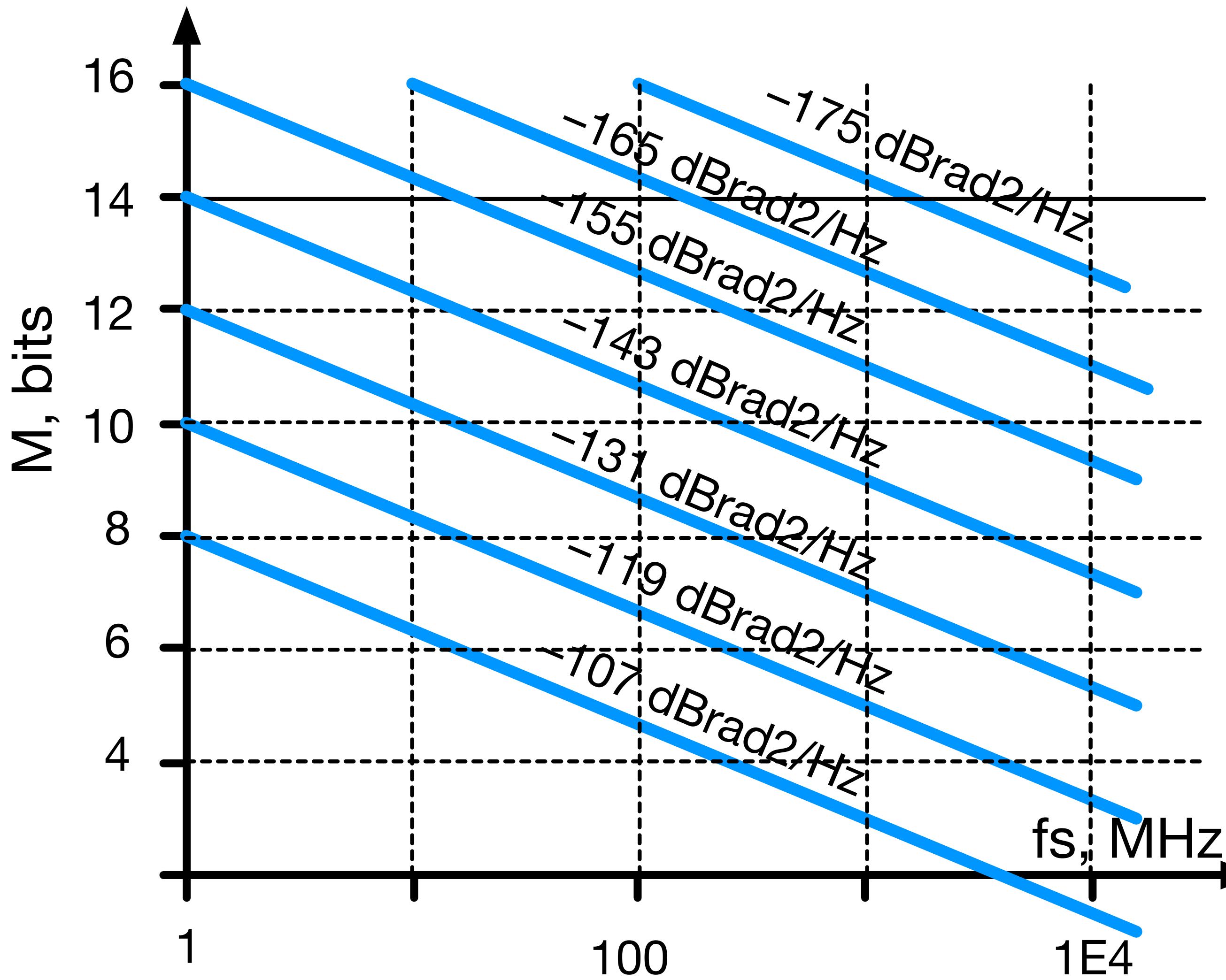
Phase noise, $S_\varphi = b_0$ (white)

$$S_\varphi = b_0 \frac{\sigma^2}{B}, \quad b_0 = \frac{V_{LSB}^2}{V_{FSR}^2} \frac{4}{3a^2 f_s}$$

$$b_0 = \frac{1}{(2^M)^2} \frac{4}{3a^2 f_s}$$

Phase Noise

Clock jitter not included



$$b_0 = \frac{1}{(2^M)^2} \frac{4}{3a^2 f_s}$$

6 dB reduction costs either

- One additional bit
- Factor of 4 higher f_s

Best results are obtained with the fastest 16 bit converters

Selected ADCs

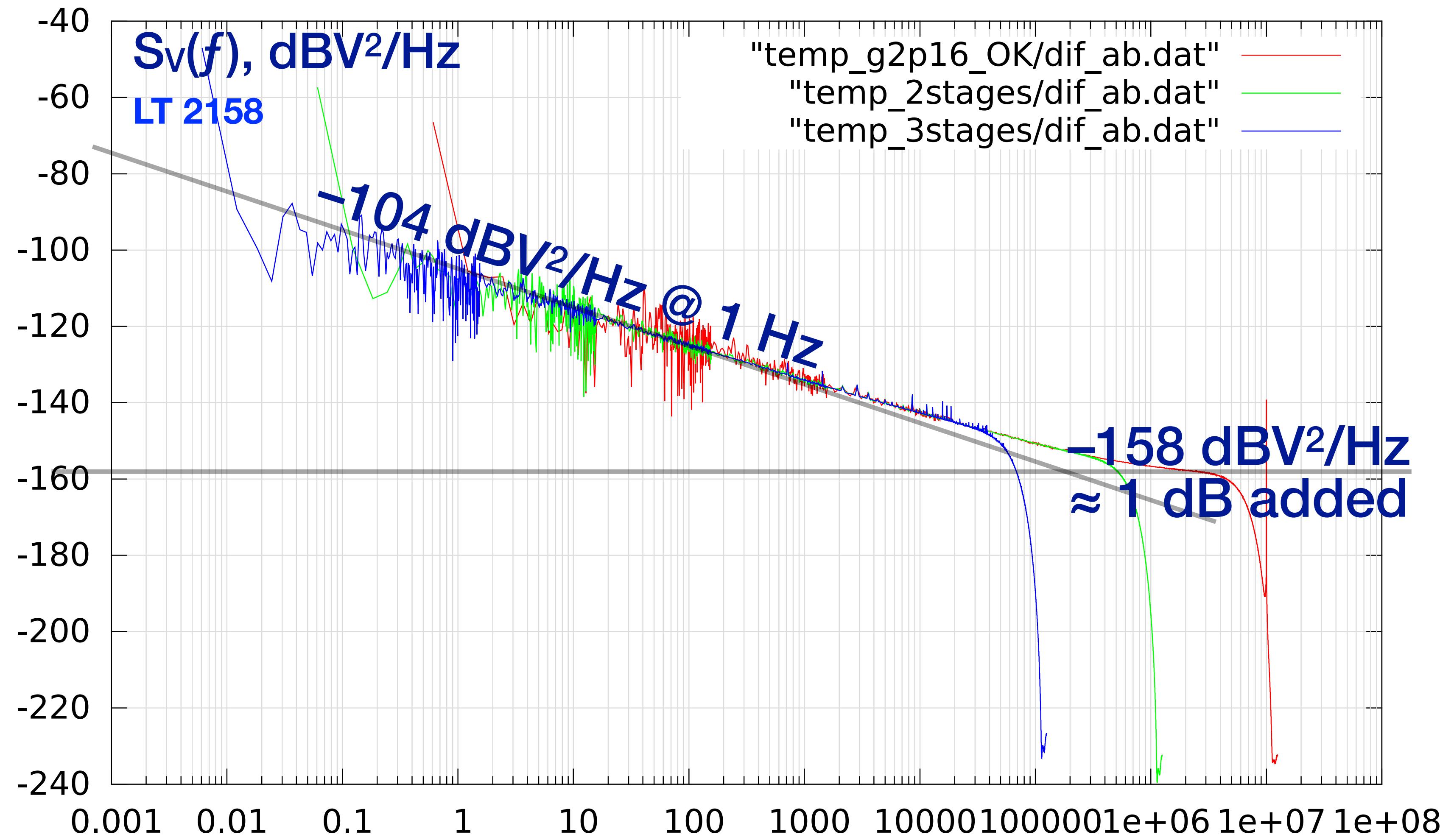
ADC type	AD9467 / Single Alazartech board)	LTC2145 / Dual Red Pitaya board	LTC2158 / Dual Eval board
Platform	Computer	Zynq (onboard)	Zynq (separated)
Sampling f	250 MHz	125 MHz	310 MHz
Input BW	900 MHz	750 MHz	1250 MHz
Bits / ENoB	16 / 12	14 / 12	14 / 12
Expected noise ($2 V_{fsr}$)	-158 dBV²/Hz	-155 dBV²/Hz	-159 dBV²/Hz
Delay & Jitter	1.2 ns & 60 fs	0? & 100 fs diff 0? & 80 fs single	1 ns & 150 fs
Power supply	1.8 V & 3.3 V 1.33 W	1.8 V 190 mW	1.8 V 725 mW

Dissipation is relevant to thermal stability

For reference, 100 fs jitter is equivalent to

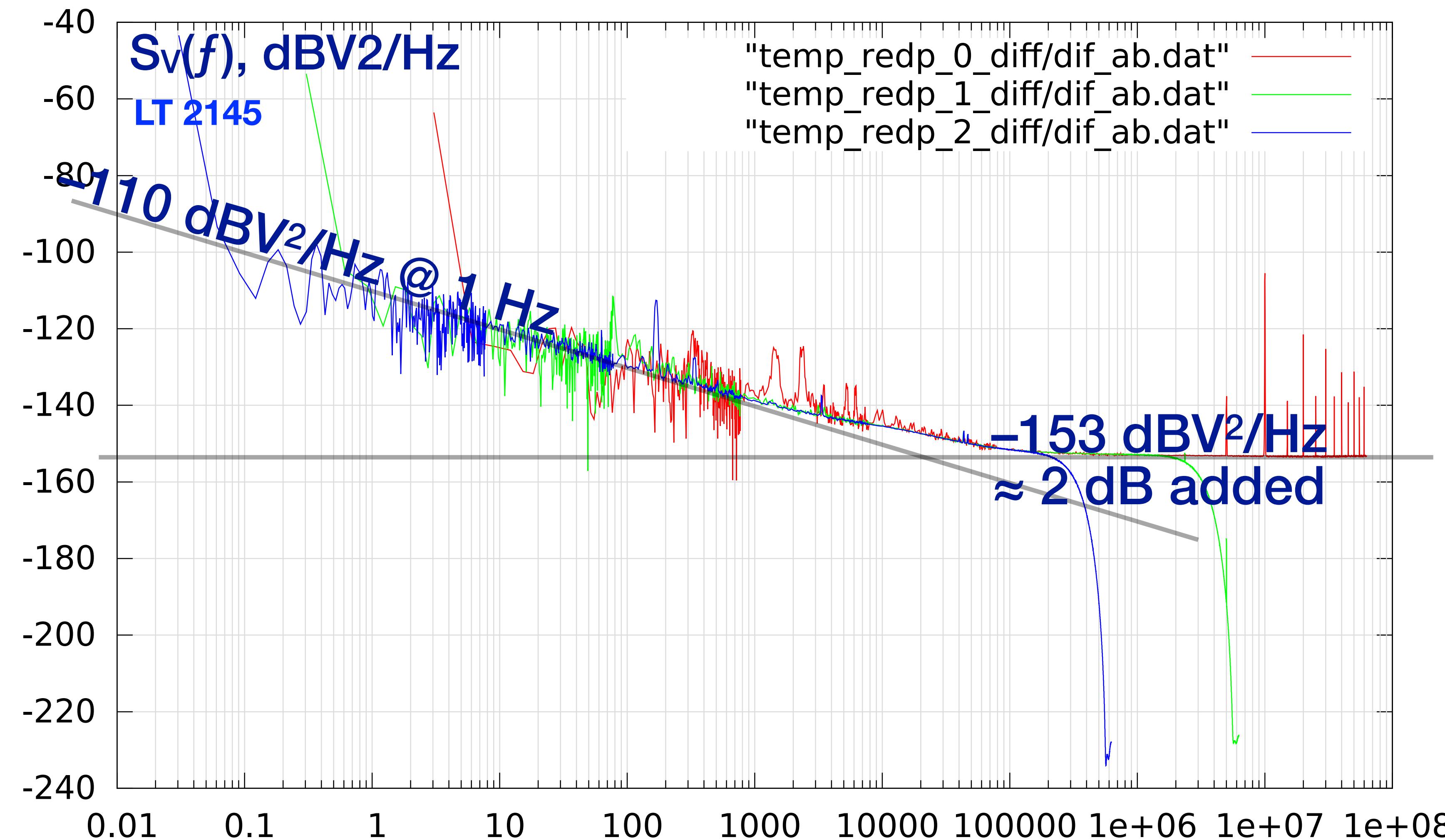
carrier f	φ rms	$S\varphi(f) = b_0$	$10 \log_{10}[L(f)]$
10 MHz	6.3 μ rad	$4 \times 10^{-18} \text{ rad}^2/\text{Hz}$	-177 dBc/Hz
100 MHz	63 μ rad	$4 \times 10^{-17} \text{ rad}^2/\text{Hz}$	-167 dBc/Hz

LT 2158 Noise



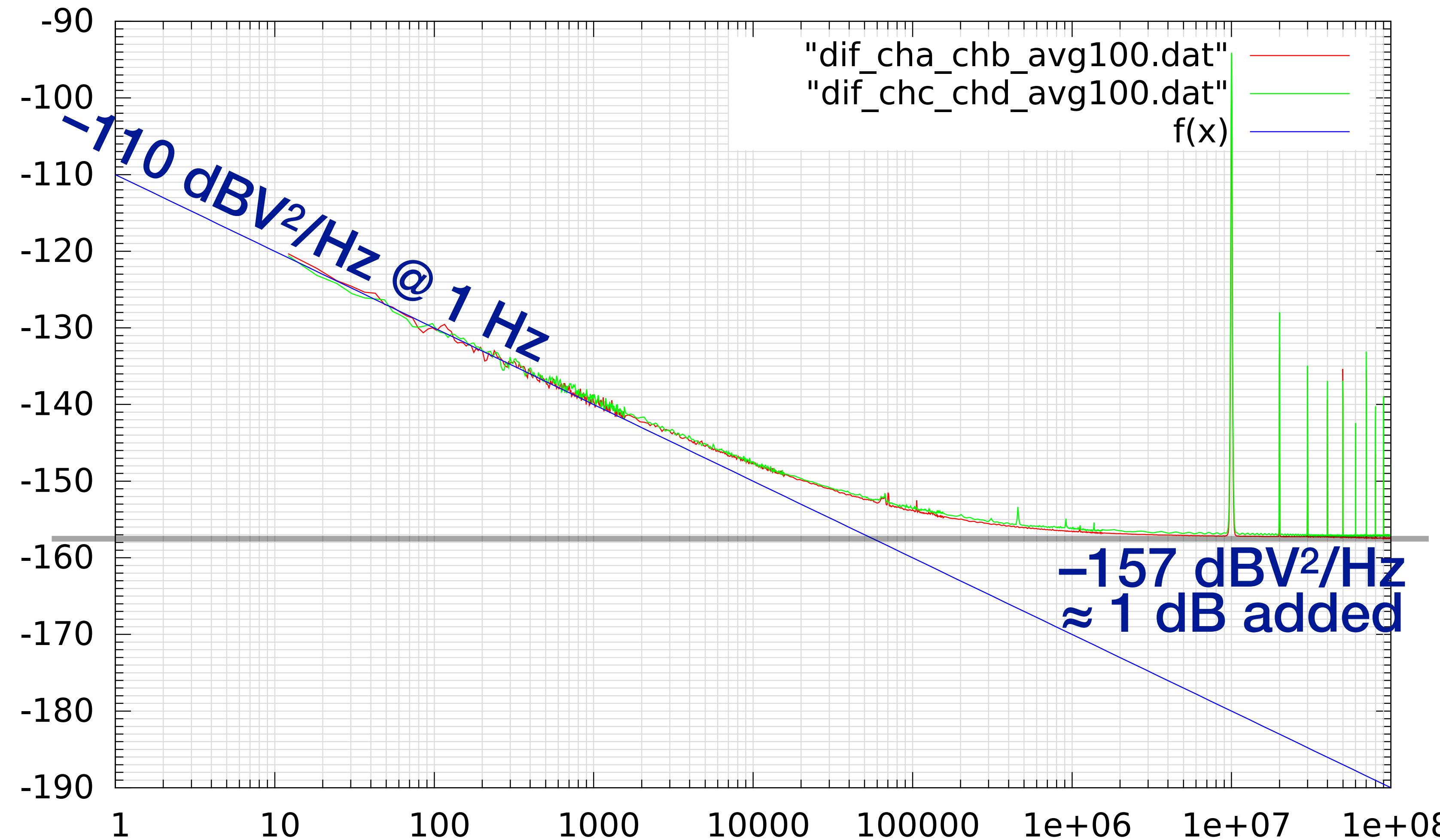
10 MHz, $V_{\text{pp}} \approx 0.95 V_{\text{FSR}}$

LT2145 (Red Pitaya) Noise



10 MHz, $V_{\text{pp}} \approx 0.95 V_{\text{FSR}}$

AD9467 (Alazartech) Noise



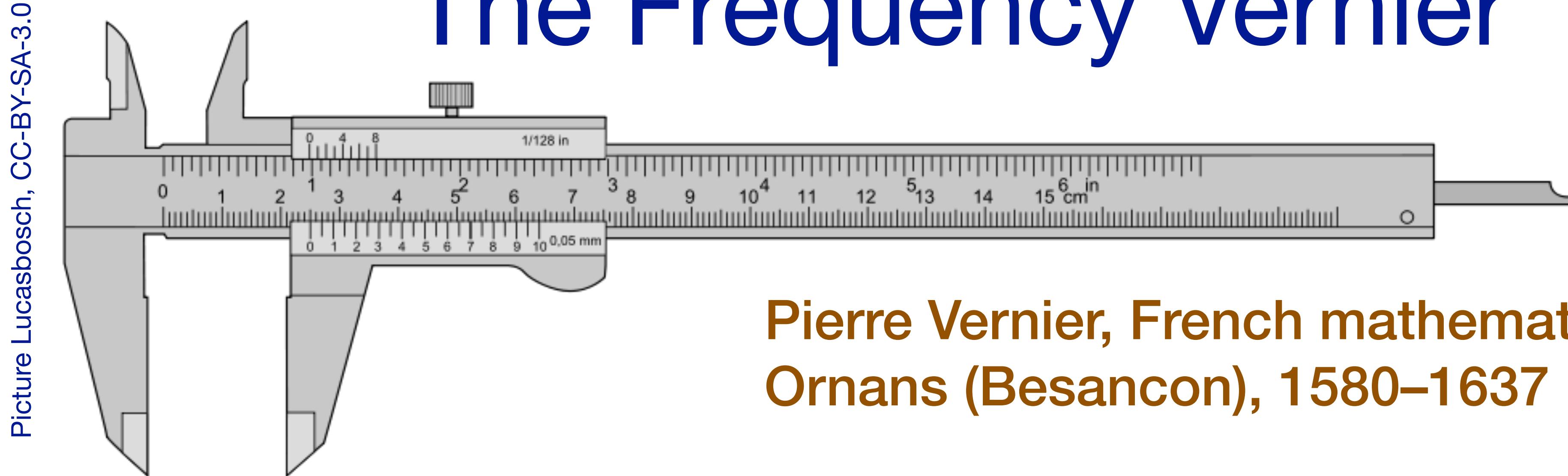
10 MHz, $V_{\text{pp}} \approx 0.95 V_{\text{FSR}}$

Time-To-Digital Conversion

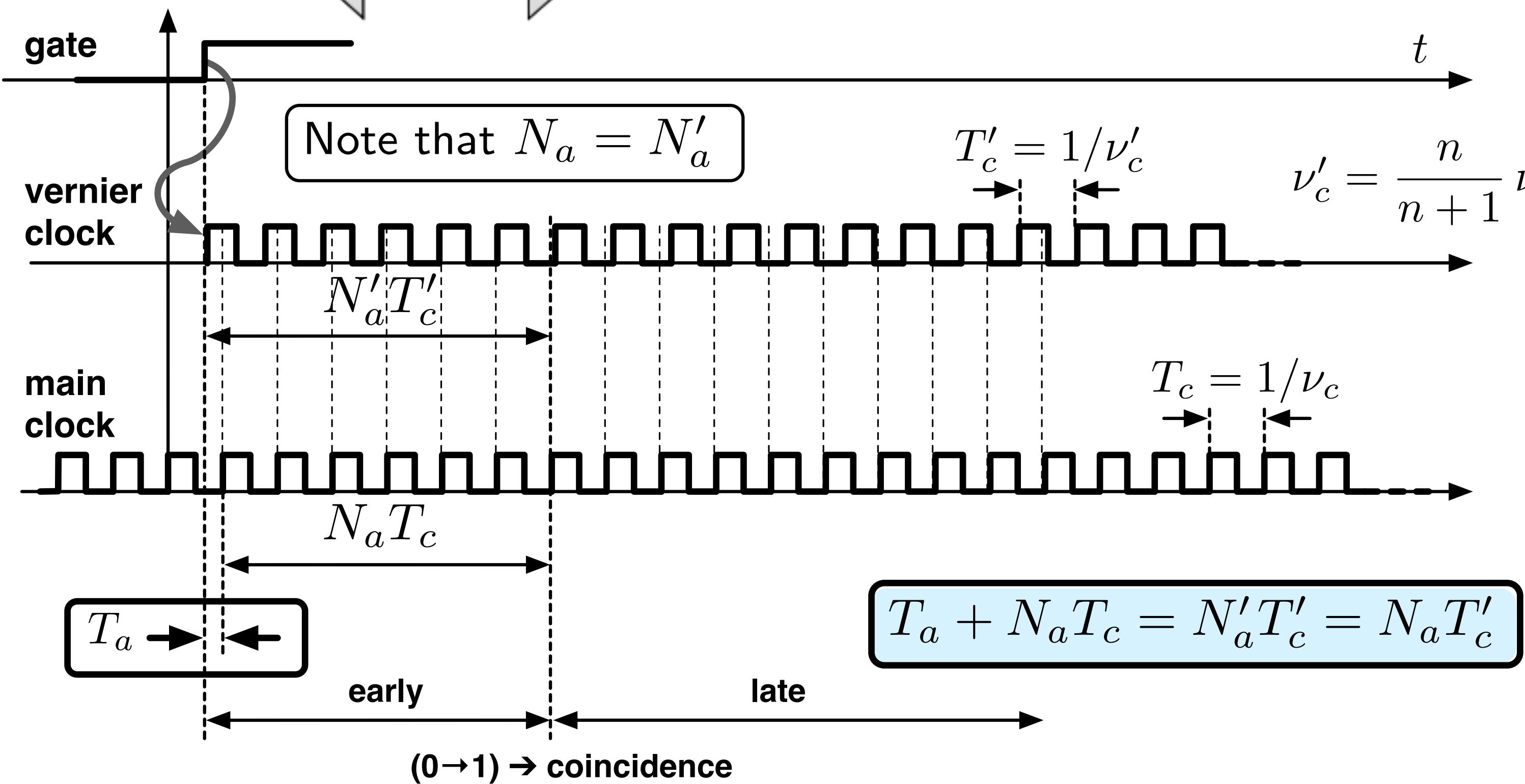
Count clock cycles (trivial)

Measure the fraction of clock cycle (next)

The Frequency Vernier



Pierre Vernier, French mathematician
Ornans (Besancon), 1580–1637



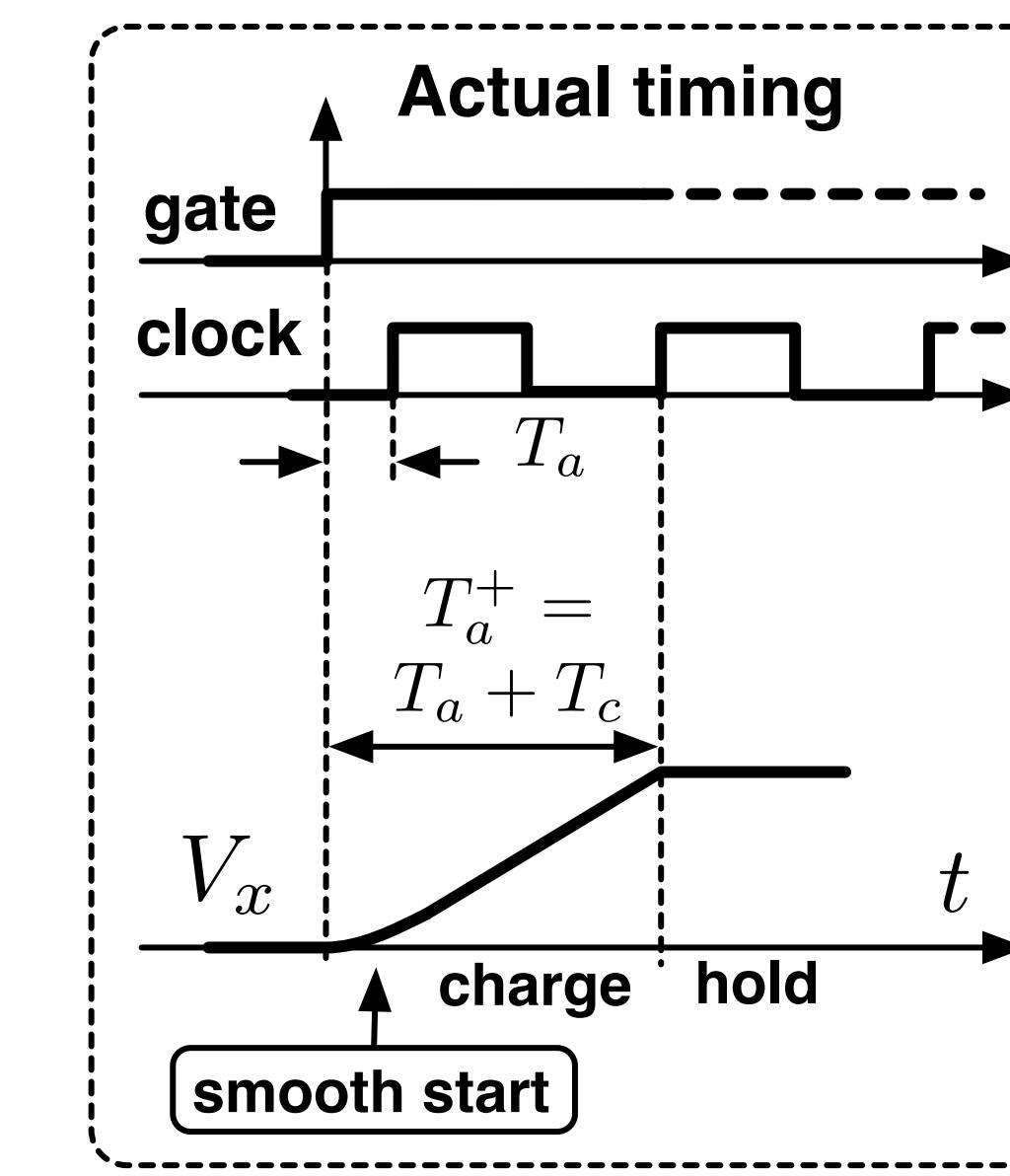
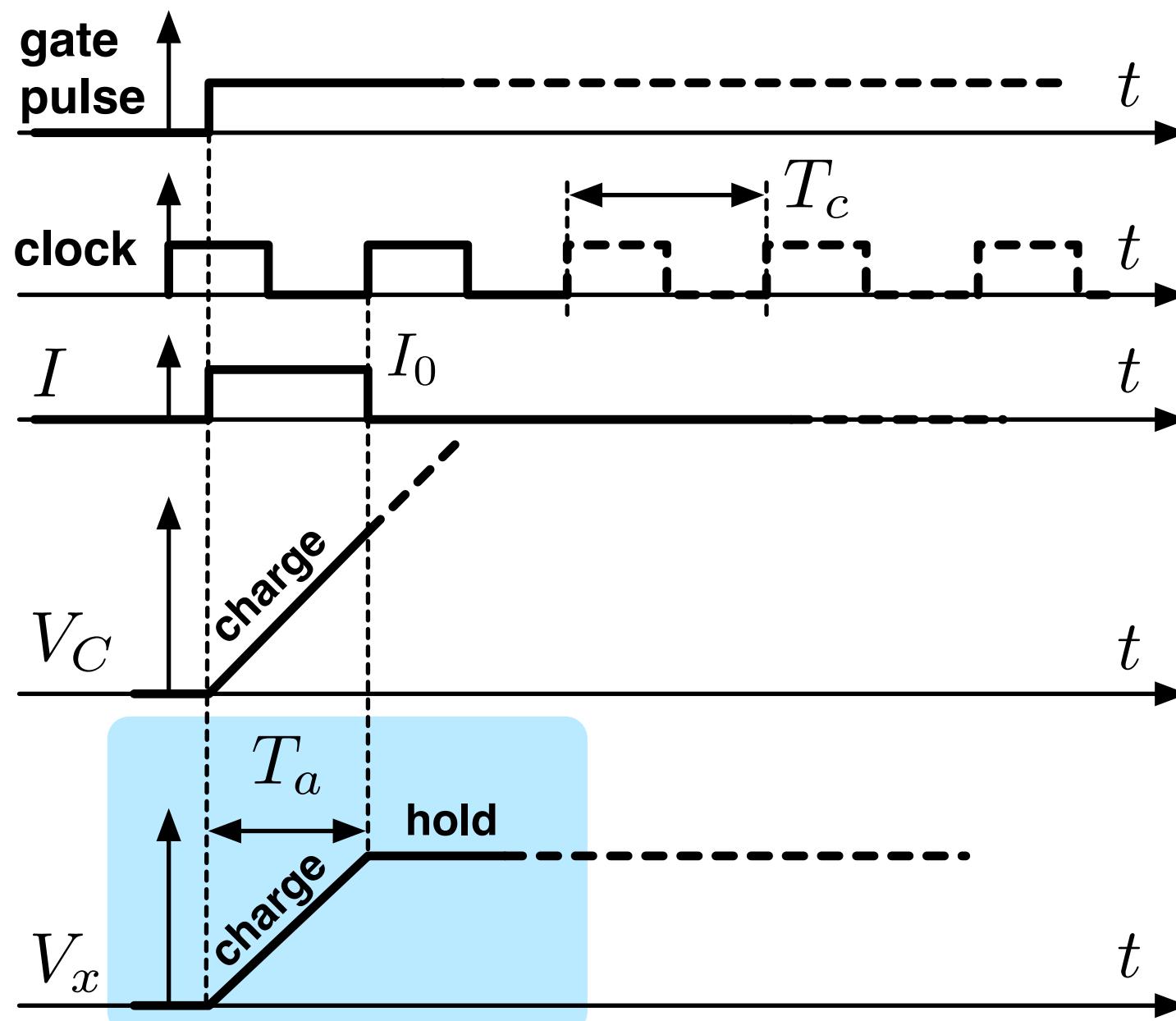
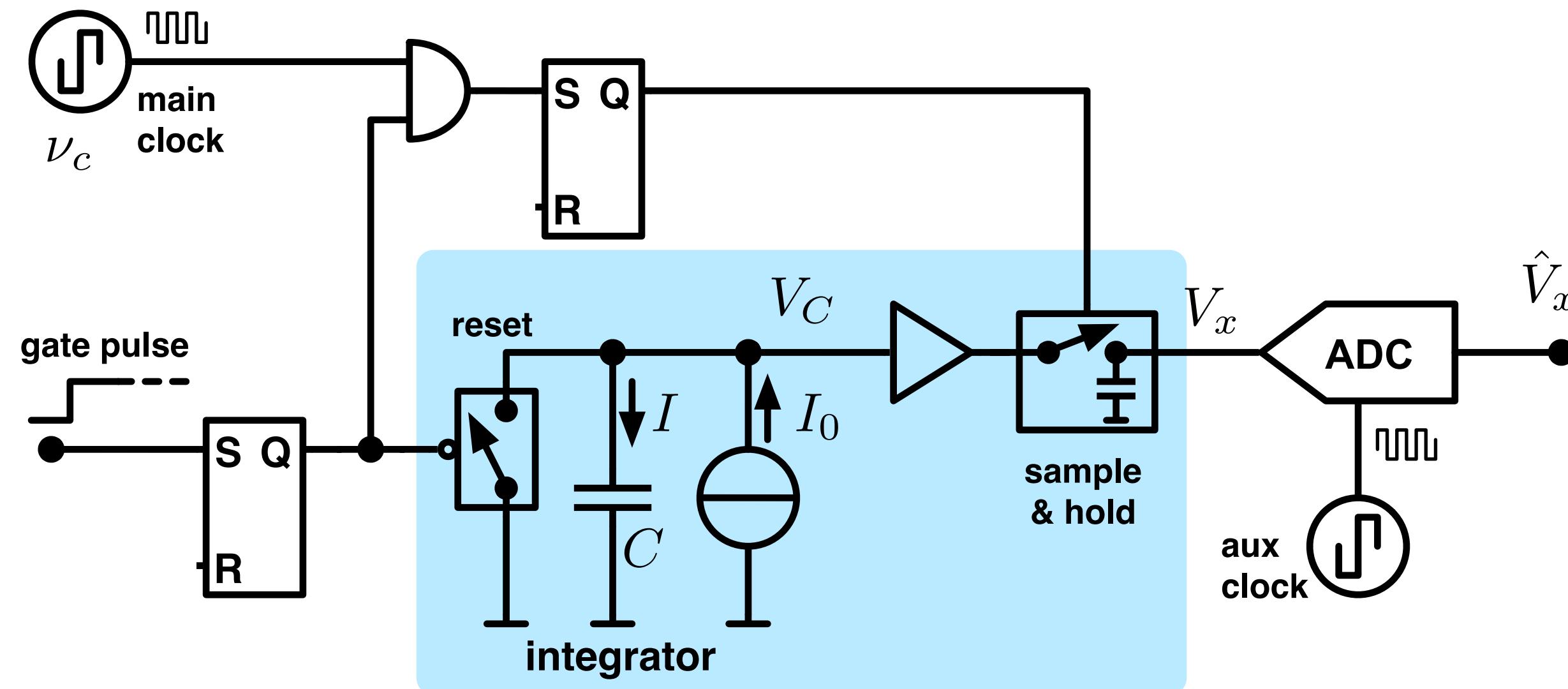
Example (HP5370A)

$$f_c = 200 \text{ MHz (5 ns)}$$

$$n = 256$$

$$1/257 \times 5 \text{ ns} = 20 \text{ ps}$$

The Ramp Interpolator



Example (Stanford SR620)

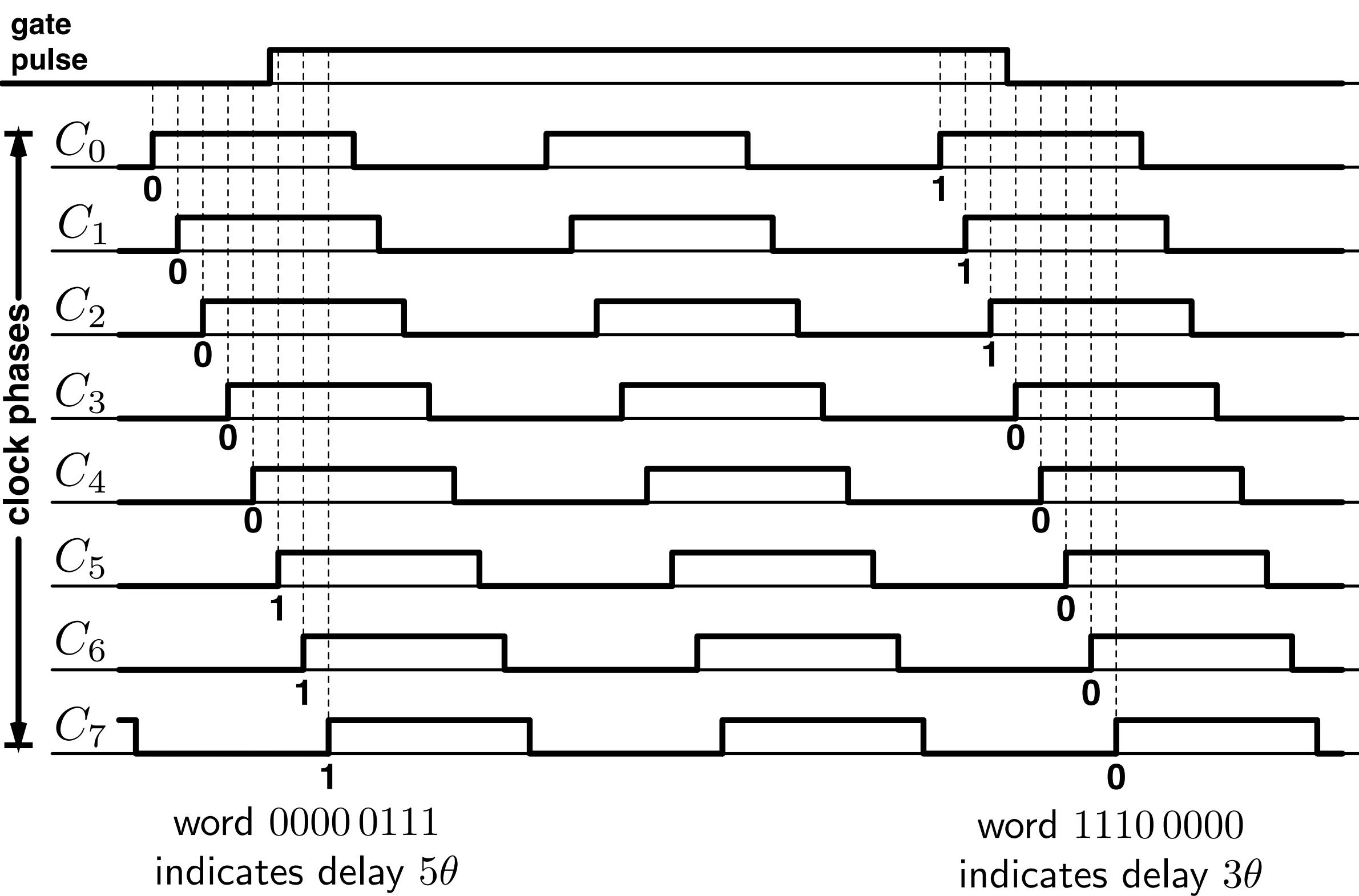
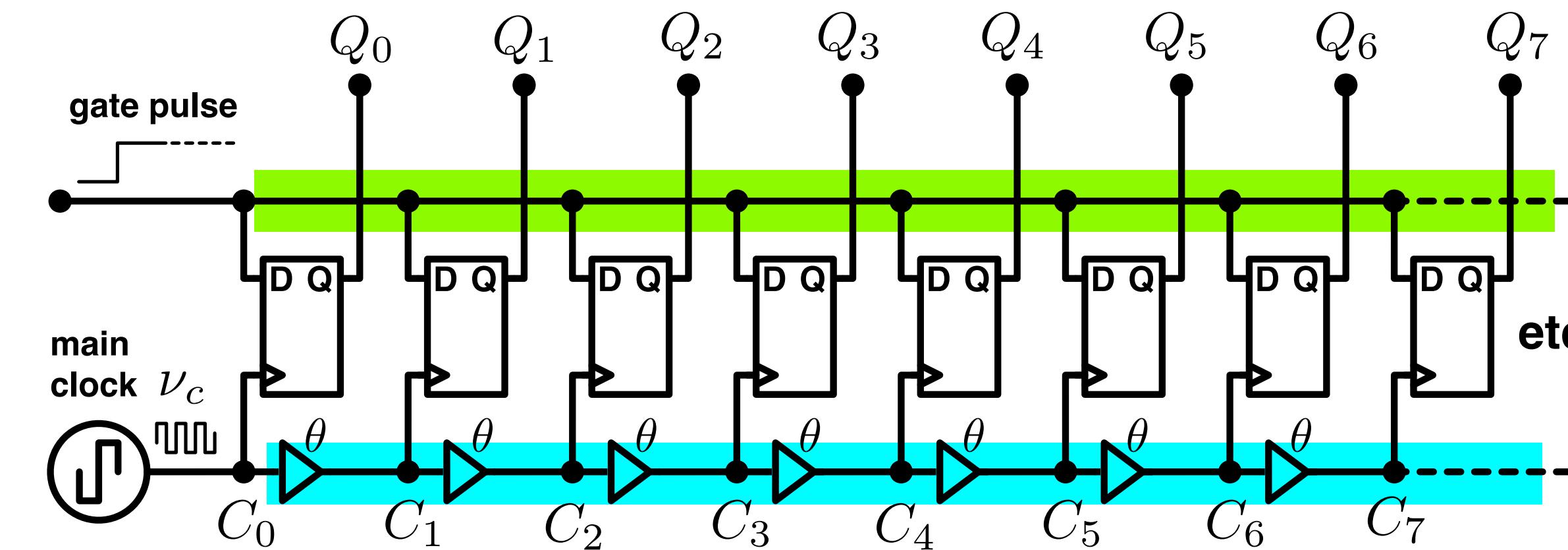
$f_c = 90 \text{ MHz} (\tau_c = 11.1 \text{ ns})$

11 bits

$\tau_c / 2^{11} = 5.4 \text{ ps}$

This costs 1 bit
ADC resolution
loss

Thermometer-Code Interpolator



Also called Multi-tapped delay-line interpolator

FPGA implementation

- Needs full layout control
- The pipeline may not fit in a cell

Great for ASIC implementation

Vernier (enhanced resolution) version

- Delay is on both lines is inevitable
- Just exploit it

$$\theta_{\text{eq}} = \theta_{\text{ck}} - \theta_{\text{in}}$$

Review article:

J. Kalisz, Metrologia 41 (2004) 17–32

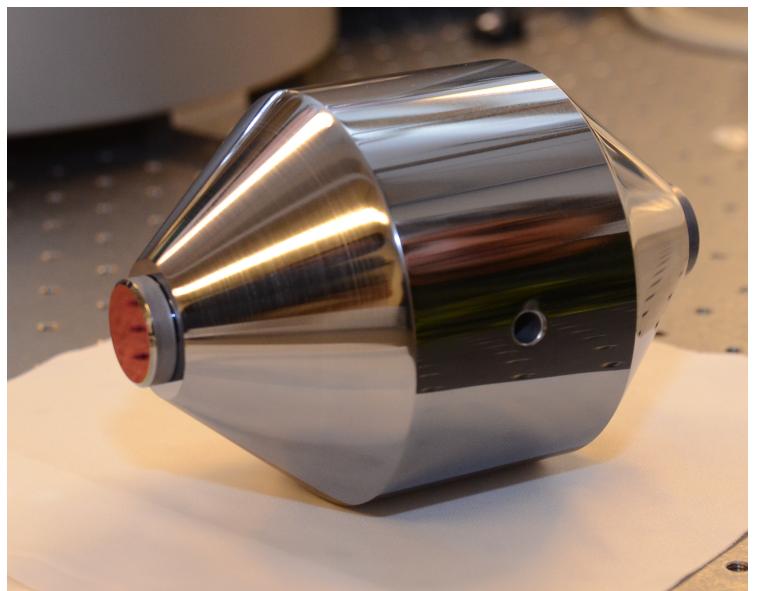
Some Examples

Carmel	NK732	3 ps	PCI/PXI time stamp	
Guide Tech	GT667/668	1 ps	PCI/PXI time stamp	
Keysight	53230A	20 ps	Lab instrument	Frequency vernier
Lange Electronic	KL-3360	50 ps	Π / Λ , special purpose	Ramp
Lumat			PCI card	Thermometer code
Stanford	SR620	25 ps	Lab instrument	Ramp
Serenum	TDC	6 ps rms	PCB module	FPGA Thermometer code
AMS Group	TDC GPX	22 ps	Chip	
MAXIM	MAX35101	8 ps	Chip	
SPAD Lab	TDC Module		Packaged module	
Texas	THS788	8 ps	Chip	Thermometer code

...And Something More

Oscillator Instability Measurement Platform⁶³

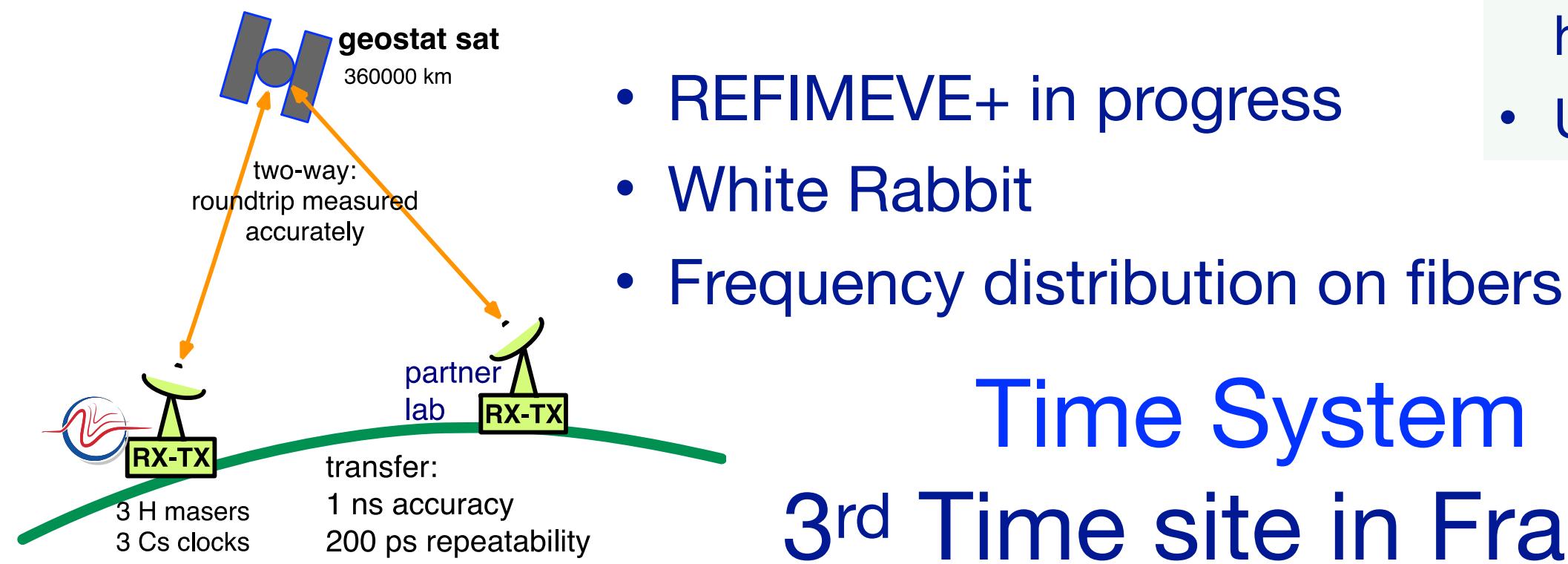
Microwave photonic oscillators



- Si Monocrystal FP, Bragg mirrors
- 17 K natural turning point
- Projected stability $3\text{E-}17$
- First tests

Also

- Spherical FP cavity, $1\text{E-}15$ stability
- Compact FP cavity, A3 size breadboard

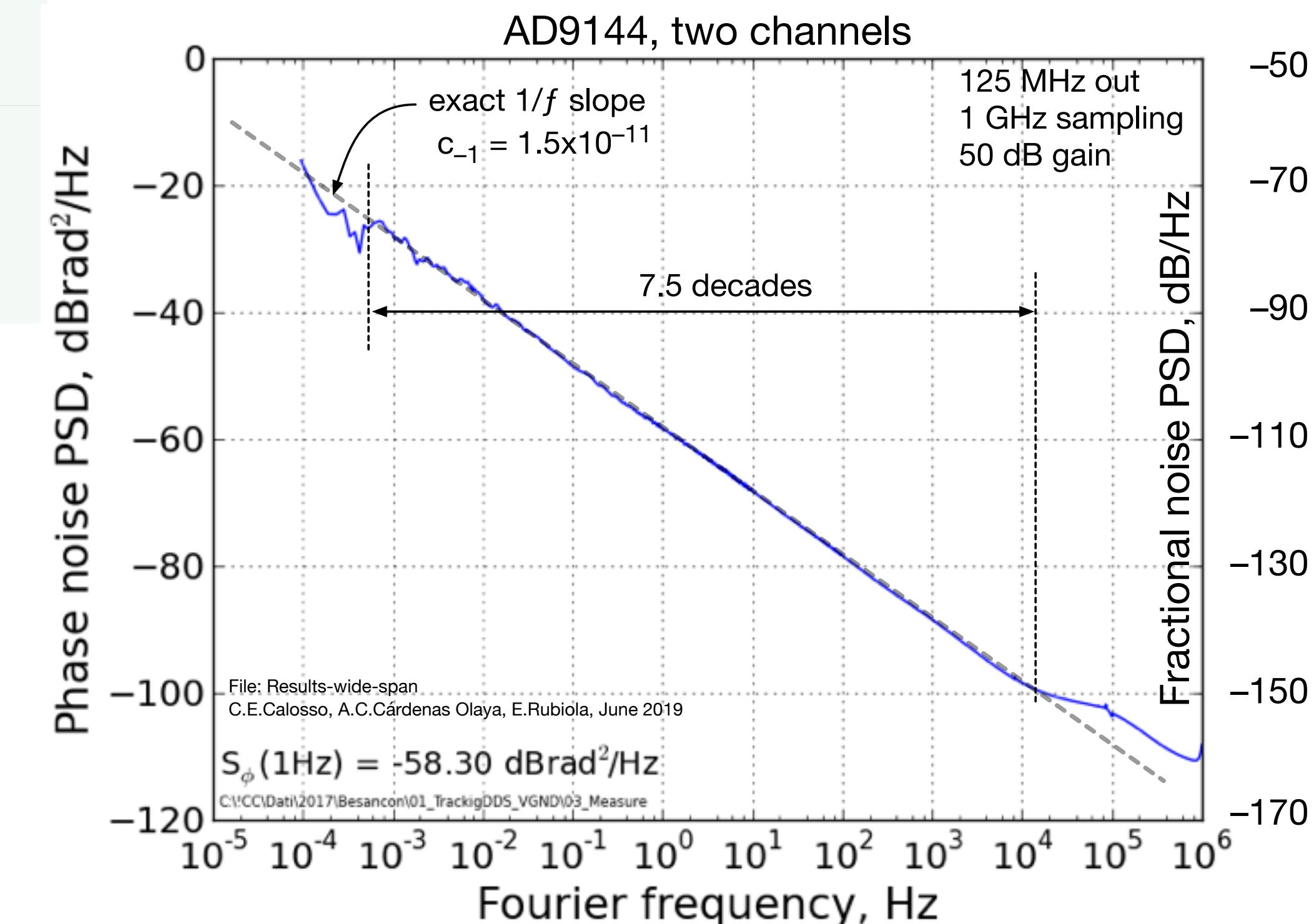
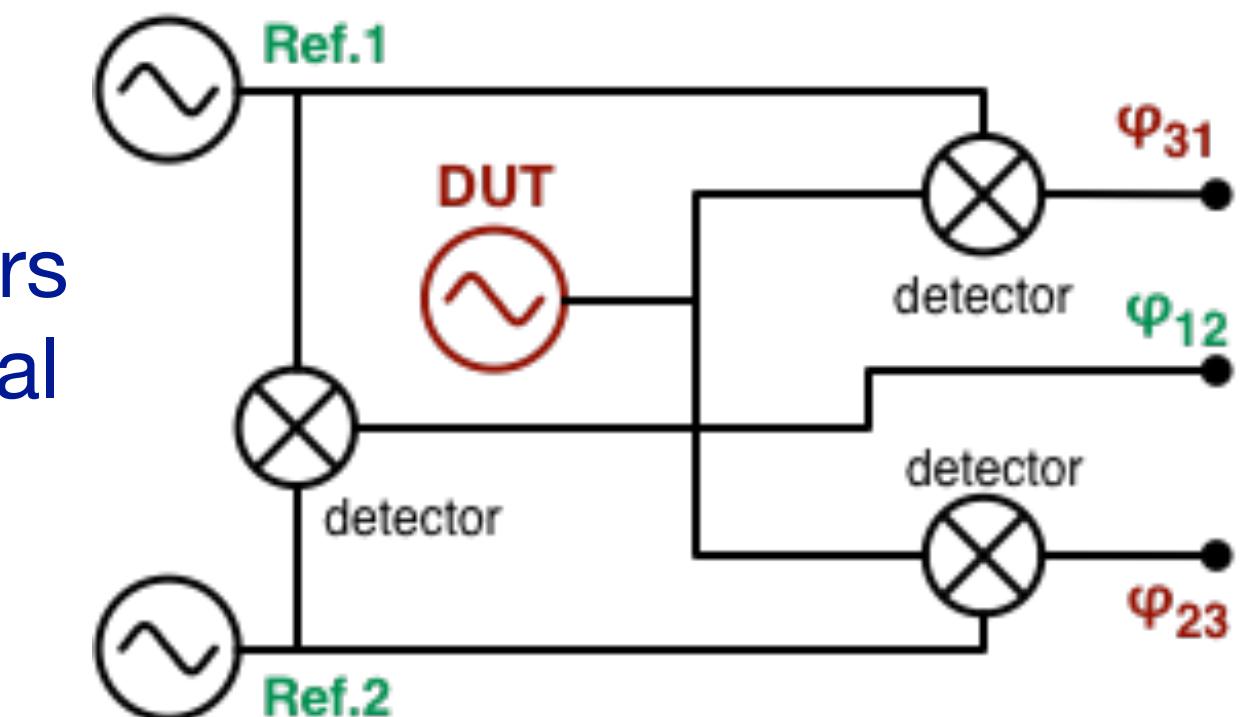


Time System 3rd Time site in France

- 3 H masers & 3 CS
- TWSTFT
- Common view GPS

Digital Electronics & Metrology

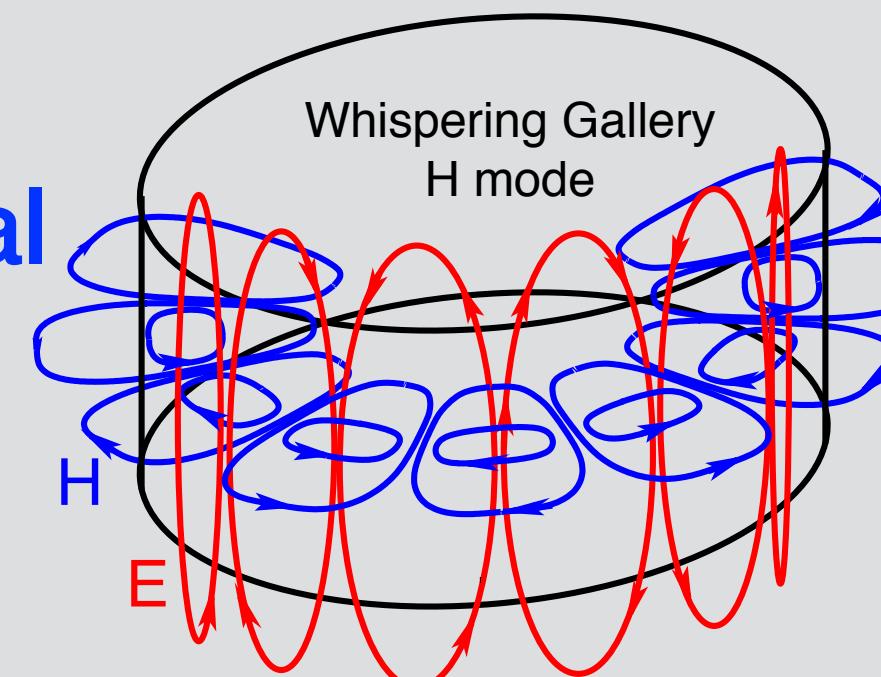
Three-cornered hat noise measurements



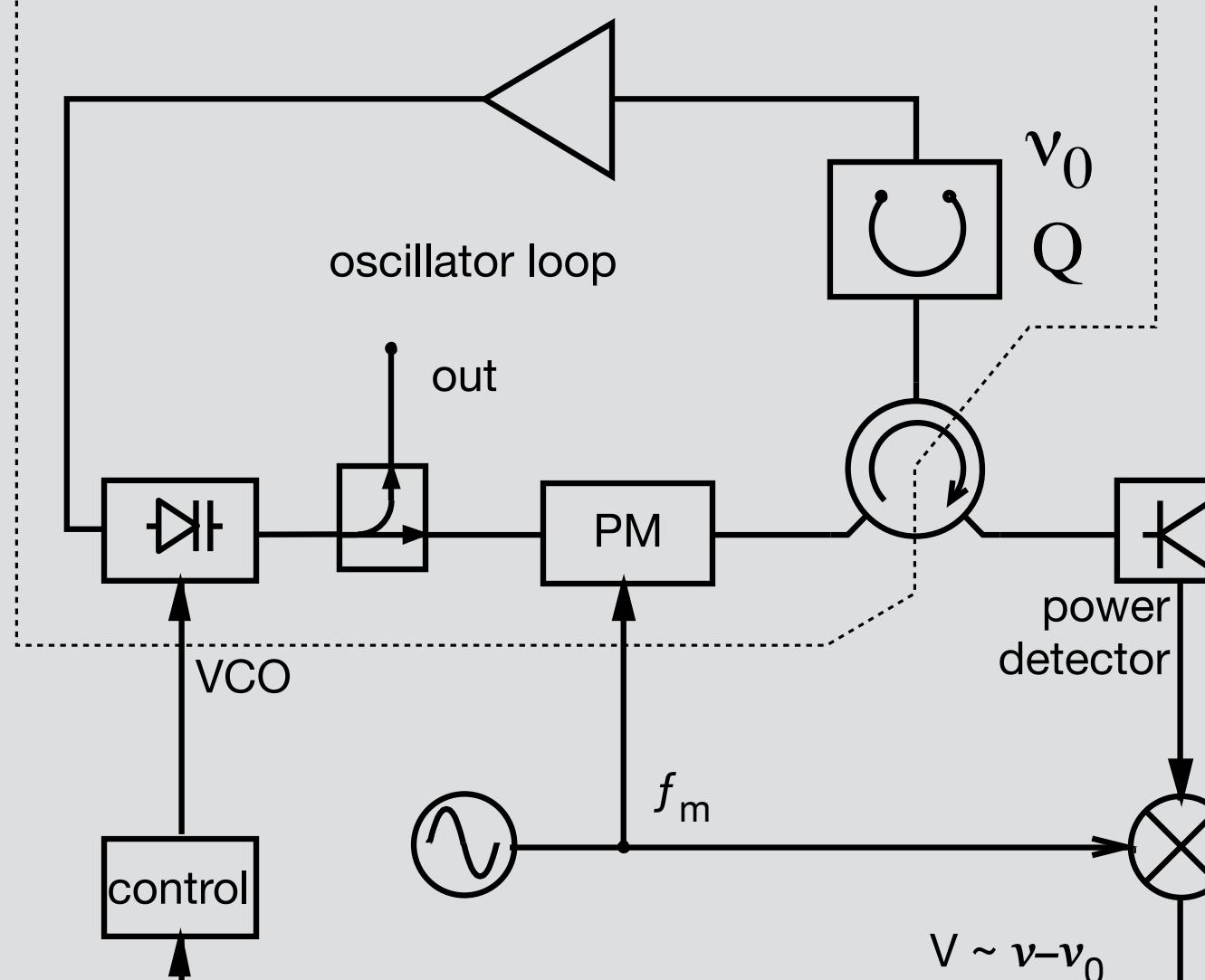
Liquid-He Sapphire Oscillator

Cr^{3+} Fe^{3+} doped
 Al_2O_3 mono crystal
 $\phi \approx 5 \text{ cm}, H \approx 3 \text{ cm}$

10 GHz resonance
 $Q \approx 2 \times 10^9$ at 5–7 K

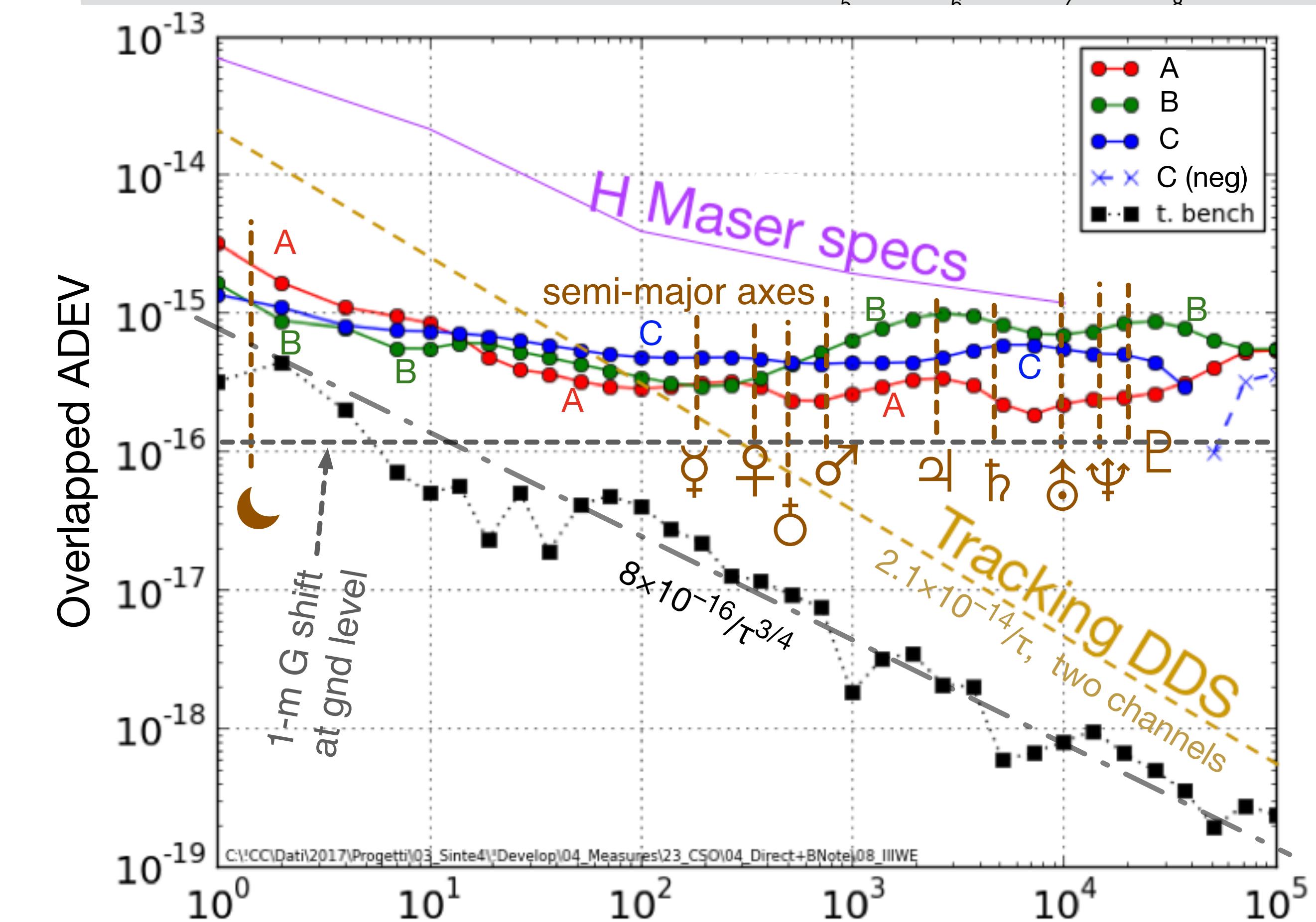
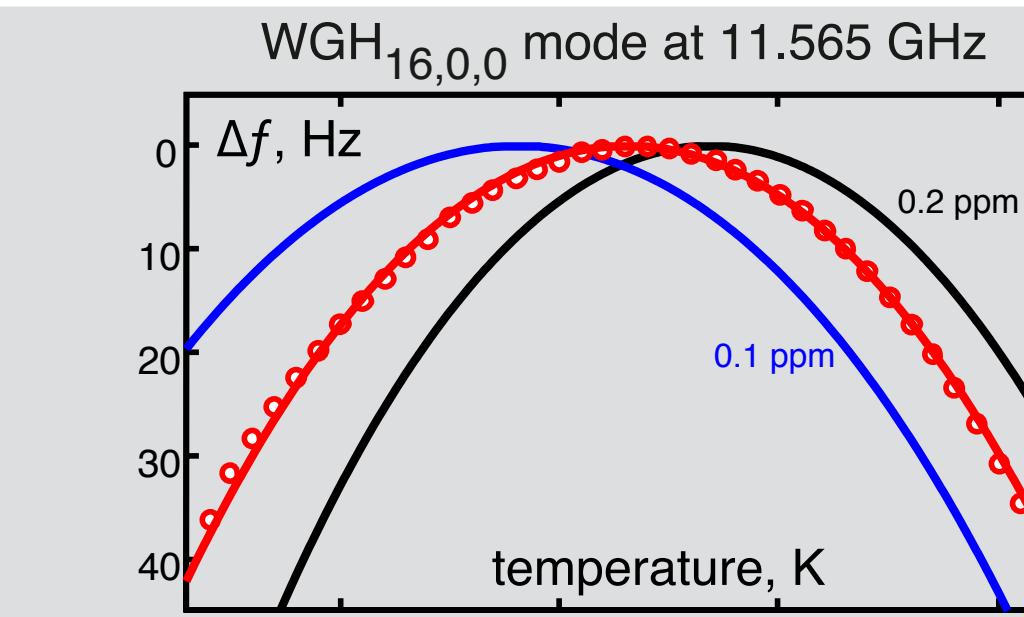


Pound-Galani Oscillator



- Pound frequency lock to the cavity
- The same cavity is used in the VCO

Paramagnetic temperature compensation





- Crash course on T&F for newcomers
- Oscillators, measurement, atomic standards, time scales, and general topics
- Broad target audience: PhD/PostDoc Students, Academics, Private Company Engineers
- Balance between academic and applied issues
- Instructors from leading European institution
- Plenary lectures 23 H, labs 12 H in small groups
- Capped no of participants, set by the labs

Every year in Besançon, end June / beginning July

<http://efts.eu>

Tentative Schedule
June 29 to July 3, 2020

